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CONTENTS

A 6-bit Bias-free Pipelined ADC with Open-loop Amplifiers

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Abstract

This paper proposes a 6-bit 160 MS/s bias-free pipelined ADC with open-loop amplifiers. The amplifiers utilize MOS transistors in triode region instead of resistors and current sources to decrease the process variation and the need of bias circuits. The amplification managed with the global-gain-control loop which realizes the error amplifier with a comparator in low-bandwidth preventing the requirement of bias current sources in linear amplification. This bias-free ADC is designed with a CMOS 0.18 μm technology and the active area is 0.7 mm^2. The circuit adopts 1.2 V for core circuits and 1.8 V for clocking with power dissipation of 90 mW. Post-layout simulation results indicate that the SNDR and SFDR achieve 35.6 dB and 40.5 dB, respectively. The maximum INL and DNL are 0.8 LSB and -0.92 LSB, respectively.

Key words: pipelined ADC, open-loop amplifier, gain control, bias-free.

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1. Introduction

The analog-to-digital converter (ADC) acts as an important role between the continuous-analog worlds with the discrete-digital fields. Recently, high-speed serial link systems such USB and SATA perform digital communication above giga-Hz [1-3]. In such high frequency operation, many digital techniques are processed after the ADC to overcome the induced noises and interferences. With the tremendous progress in the chip process technology, the scaling technique has driven the operating clock of digital computation toward higher frequency. It is a significant subject to investigate the novel technique of developing high-speed ADCs for the speedy communication. ADCs with flash architecture perform the highest speed in conversion [4-6]. Nevertheless, the power hungry property increases the power dissipation of the entire system. Pipelined architecture is economical at both power and speed in the ADC design. Nevertheless, the operation frequency of conventional approaches is limited with the closed-loop amplifiers in the pipelined ADCs. The open-loop amplification in [7][8] is successfully applied in the first stage of the high-resolution pipelined ADC with digital calibration. And [9] develops a global-gain-control loop to manage the high-speed open-loop amplification with linear error-amplifier. Based on the previous work of [9], resistors and bias current sources of the open-loop amplifiers are replaced with MOSs in triode region in this work. Furthermore, the linear error-amplifier is substituted for a latch-type comparator. Consequently, the designed 6-bit pipelined ADC operates at 250-MS/s without the need of additional bias circuits.

2. Circuit Description

2.1.System Architecture

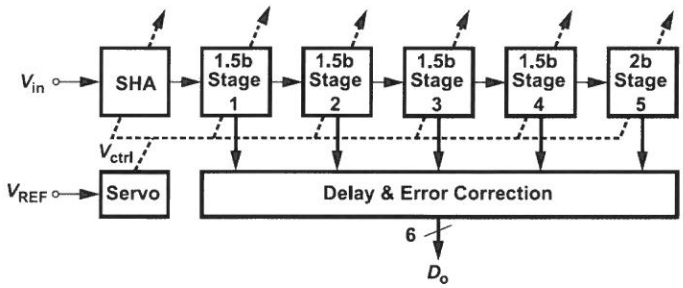


Figure 1. System architecture.

The architecture of the proposed 6-bit pipelined ADC is depicted in Fig.1. This ADC consists of a sample-and-hold amplifier (SHA), four-1.5b stages, and a 2b-flash stage. The global gain control servo provides the control voltage to compensate the gain error of the pipelined stages. After the delay alignment and the digital error correction, 6-bit digital data are obtained at the output.

2.2.Open-loop Amplifier

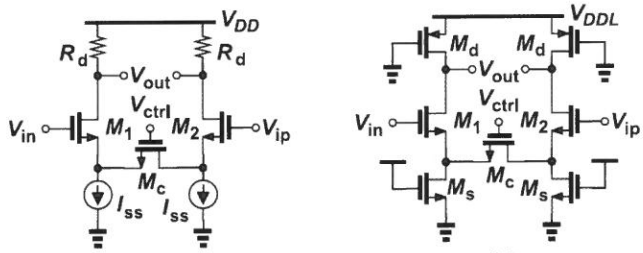


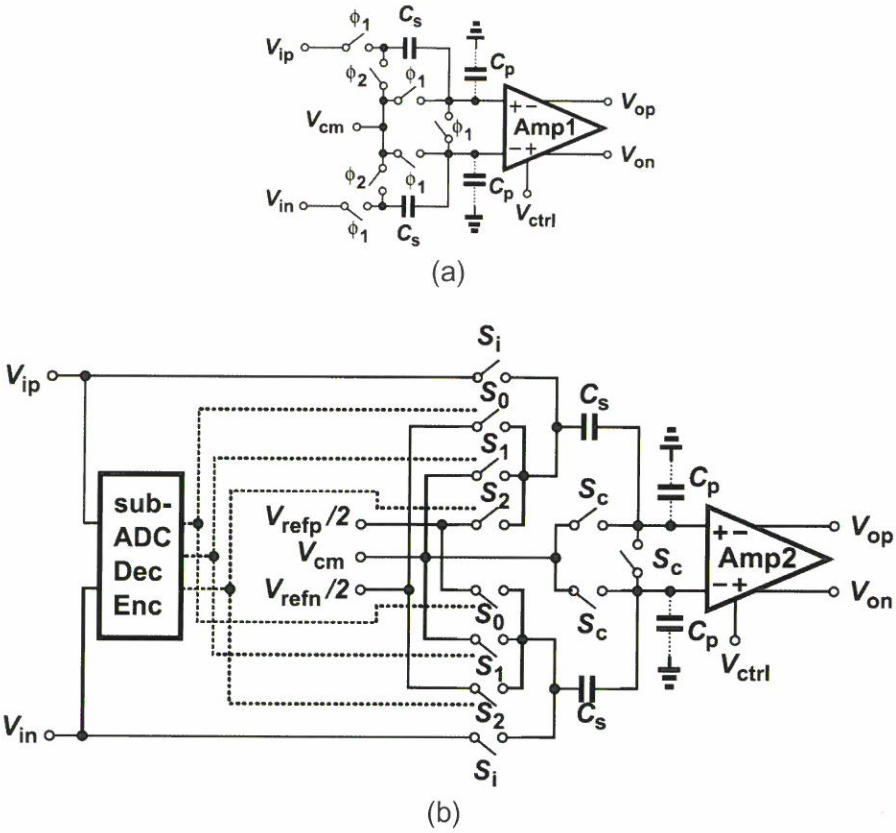
Figure 2. (a) The open-loop amplifier in previous work [9].
(b) The proposed open-loop amplifier.

The previous work [9] employs the open-loop amplifier of Fig. 2(a) in the pipelined stage. The resistors suffer from process variation and occupy larger circuit area [10]. Moreover, the bias current requires additional routing in managements and the design of bias circuits. In this work, the low-gain amplifier utilizes MOS transistors biased at deep-triode region to replace the resistor and the current sources as depicted in Fig. 2(b). To lower the power consumption and to provide a proper voltage level for biasing, the supply voltage is down to V_{DDL} of 1.2 V. The MOS transistors biased at deep-triode region are achieved with connecting the gates of M_ds to the ground and tying the gates of M_ss to V_{DDL} without additional bias voltages. As M_c operates at triode region, the small signal analysis of this common source amplifier with source degeneration is given by

$$|A_v| = \frac{g_m R_d}{1 + g_m\left(R_s \| R_c/2\right)}, \tag{1}$$

where R_d, R_s, and R_c are the ON resistance of M_d, M_s, and M_c, respectively [11][12]. Due to the open-loop operation, the overall gain is altered by the input parasitic capacitive division. To compensate this unknown gain reduction, the gain of the open-loop amplifier must be tunable. Because the gain of the amplifier is related to R_c, varying R_c with the V_{ctrl} alters the gain of the open-loop amplifier. The V_{ctrl} is provided with the global gain control servo and will be discussed in subsection 2.5.

2.3.Sample-and-hold Amplifier and Pipelined Stage



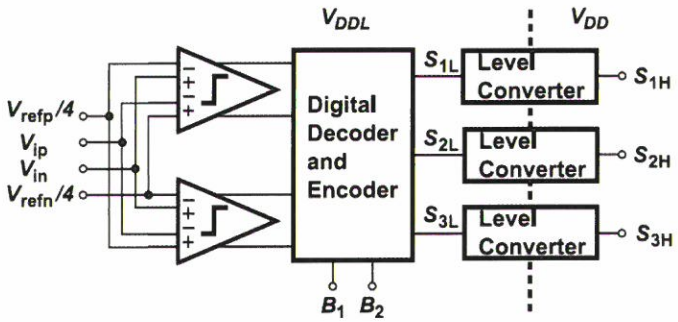
(a)

(b)

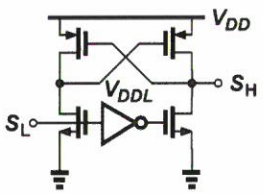
Figure 3. (a) Sample-and-hold amplifier. (b) Pipelined stage.

At high frequency data conversion, the performance is sensitive to timing jitter. Consequently, the sample-and-hold amplifier (SHA) in Fig. 3(a) is adopted to soften the effect

of jitter with the high-frequency input signals. Two non-overlapped clocks (ϕ_1 and ϕ_2) control the switches to obtain the held signal. During ϕ_1 the input nodes of the amplifier, Amp1, are set to V_{cm}. And the differential inputs (V_{ip} and V_{in}) are stored in C_ss. When ϕ_2 is active, the stored signals are held at V_{op} and V_{on} through the amplifier, Amp1. The pipelined stage is shown in Fig. 3(b). When S_i and S_c are ON, the input signal is sampled at C_s and input nodes of the amplifier, Amp2, is set to V_{cm}. In amplification mode, the stage output is obtained from Amp2 according to the results of sub-ADC, decoder (Dec) and encoder (Enc). Nevertheless, since the charge in C_s is shared by C_p in SHA and pipelined stage, the amplifiers need to compensate this capacitive division [4]. Amp1 and Amp2 employ the identical topology in Fig. 2(b). The compensation is achieved through the global-gain control servo to obtain the over-all gain of two in the pipelined stage by adjusting V_{ctrl}. Because the ideal value of the overall gain in the SHA is unity, the gain of Amp1 in SHA is designed as the half of Amp2 in the pipelined stage. Although the over-all gain controlled with V_{ctrl} may cause the gain error in SHA, the linearity of the converter does not be influenced. This kind of gain error in ADC is easily compensated with auto gain control mechanism in digital communication systems.



(a)



(b)

Figure 4. (a) Sub-ADC block. (b) Level converter.

The sub-ADC in the pipelined stage consists of 2 comparators and some digital encoder and decoder circuit is depicted in Fig. 4(a). To have a better ON-characteristic of switches, the clocking signal operates at the standard supply voltage of 1.8 V in the 0.18 μm CMOS technology. Therefore, outputs of the digital circuit have to level up the driving capability. The level converter is achieved by the circuit in Fig.4(b) [13].

2.4.Comparator

The pipelined stage and the global gain control servo both demand four-input comparators to provide the comparison of two differential signals with two differential references. The dynamic comparator in Fig. 5 is adopted to reduce static power dissipation [14][15]. This comparator is composed of four-input differential pairs, M_1 . M_4, and a back-to-back latch, M_7~M_{10}. When ϕ_1 is low, M_5 and M_6 are OFF and four inputs pre-charge at the gates of M_1~M_4. No dc path occurs at this phase. Meanwhile, M_{11} and M_{12} are ON and the outputs of the comparator are tied to V_{DD}. As ϕ_1 goes high, M_5 and M_6 are ON and M_{11} and M_{12} are OFF. The back-to-back latch regenerates the result of the comparison at the output.

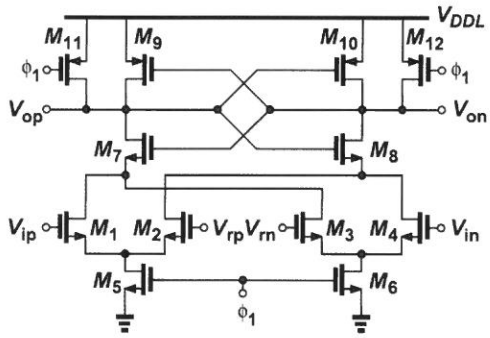


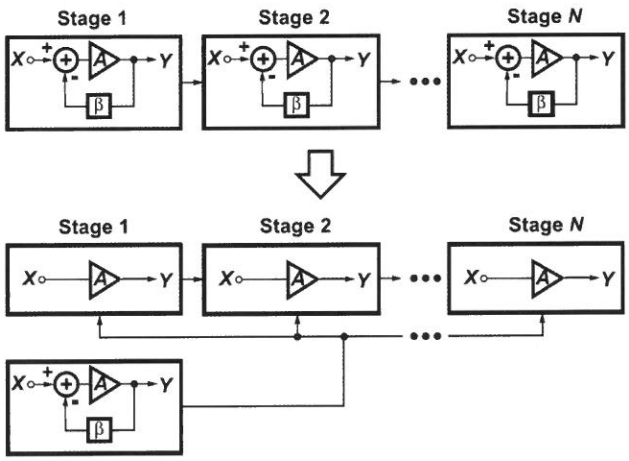
Figure 5. Comparator.

2.5.Global-gain Control

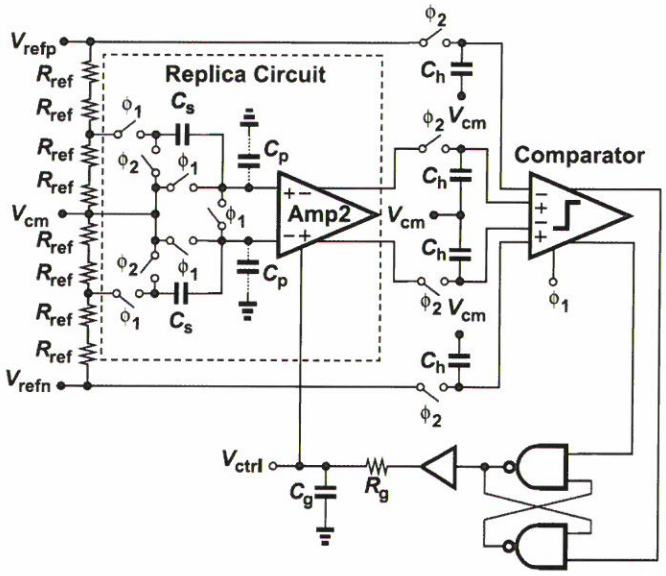
In a conventional 6-bit pipelined A/D converter design, the open-loop gain of the amplifiers in the 1.5-bit stages must be greater than 40 dB. High gain amplifiers require stringent design trade-offs between power and settling-time. In this work, open-loop amplifiers replace the conventional closed-loop amplifiers in the pipelined ADC as shown in

Fig. 6(a). The global-gain control substitutes for the individual feedback control in pipelined stages. Since the loop bandwidth of the global-gain control is not as high as the requirement in closed-loop amplifiers of conventional pipelined stages, the stringent requirement of the amplifiers in global-gain control loop is relaxed. Therefore, the pipelined ADC with open-loop amplifiers achieves high-speed conversion while the global-gain control working at lower bandwidth.

Due to the low bandwidth characteristics of the global-gain control loop, the linear error amplifier in [4] is replaced with a latch type comparator of Fig. 5 to avoid the requirement of bias current sources as depicted in Fig. 6(b). Since the comparator in Fig. 5 demands a reset phase to tie the outputs to the V_{DDL}, a NAND type SR-latch is added to sustain the result of previous comparison. At ϕ_1 state, $V_{ref}/2$ is sampled in the C_s and the input nodes of the Amp2 is reset to V_{cm}. At ϕ_2 state, the output of Amp2 is sampled and compared with V_{ref}. The output result of the comparison is generated at next ϕ_1 state. The digital-like comparator provides an infinite gain and the R_gC_g low-pass filter creates a dominate pole at the low-frequency. Consequently, this global-gain control loop maintains the over-all gain of 2 without the stability consideration. Becaue the pipelined stage is duplicated at the global gain control servo, the parasitic attenuation is almost the same. Accordingly this V_{ctrl} further connects to the pipelined stages of the converter to achieve the global-gain control.



(a)

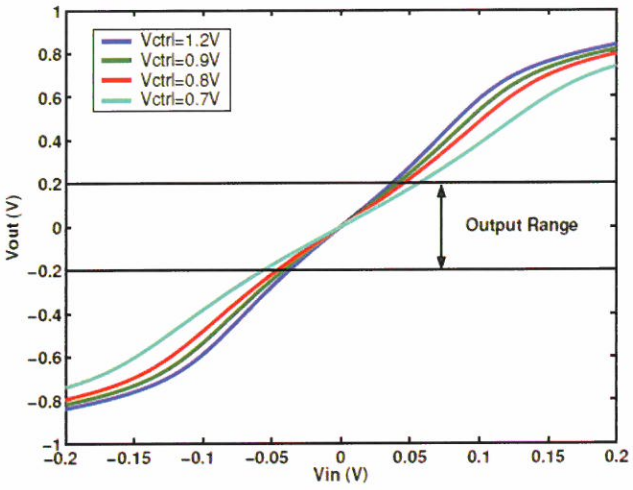


(b)

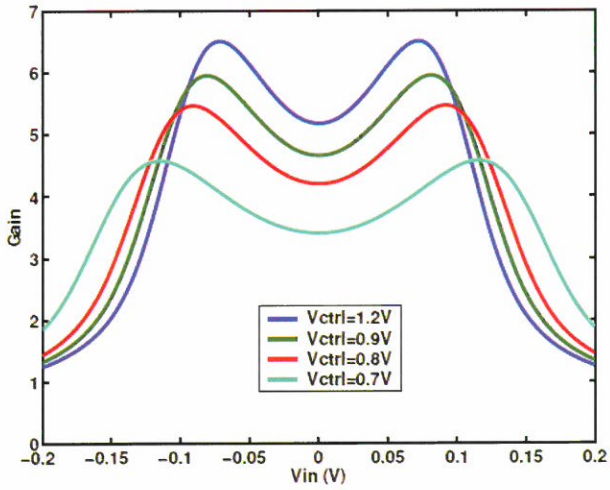
Figure 6. (a) Principle of global-gain control. (b) Global-gain control servo.

3. Simulation Results

The input-output transfer curves of the Amp2 with various V_{ctrl} are shown in Fig. 7(a). Their corresponding gain variation is depicted in Fig. 7(b). This simulation reveals that raising V_{ctrl} of M_c makes the transfer curves sharper and increases the corresponding gains. The linear output range of the transfer curve is $\pm$0.2V. Therefore, the parasitic voltage division can be compensated with the gain enhancement of V_{ctrl}.



(a)

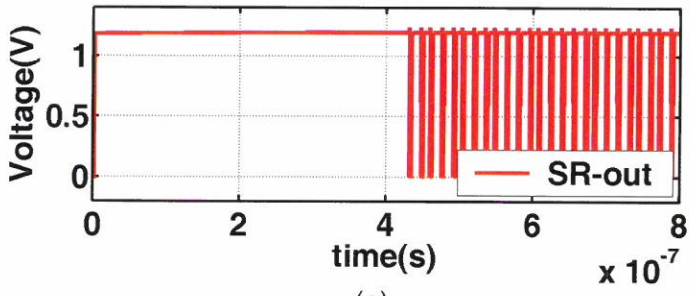


(b)

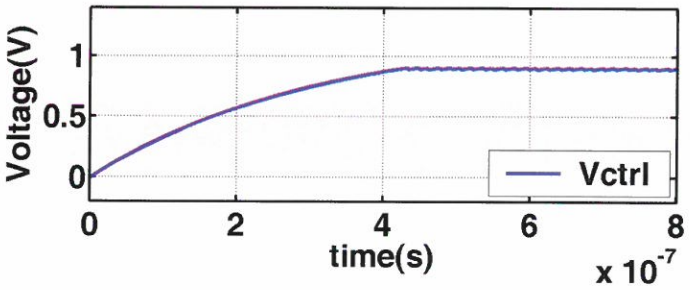
Figure 7. (a) Input-output transfer curves and (b) gain of open-loop amplifier.

The Hspice simulation results of Fig. 6(b) are shown in Fig. 8. If the initial output of LPF is 0, the gain of the open-loop amplifier is small, and the output of the SR-latch is at V_{DDL} in Fig. 8(a) because of initial comparison. In this period, the input of LPF is like a step input

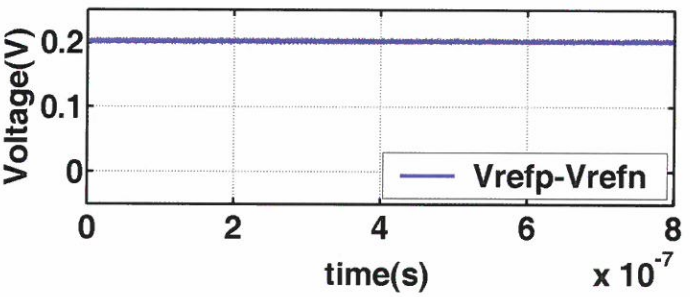
as illustrated in Fig. 8(b), and V_{ctrl} increases to enlarge the gain of the open-loop amplifier as illustrated in Fig. 8(a). When the output of amplifier, V_o , in Fig. 8(d) is near the V_{ref} as shown in Fig. 8(c), V_{ref} reaches the desired value and the SR-latch begins to toggle the comparison. Therefore, V_{ref} rapidly converge to the desired value. The simulation result indicates that V_{ref} settles within 43 μs at the R_g = 20 kΩ and C_g = 10 pF.



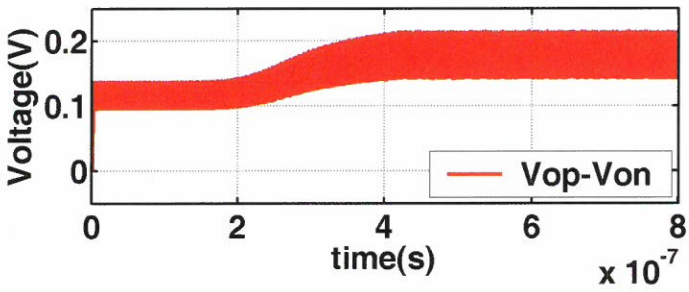
(a)



(b)



(c)



(d)

Figure 8. (a) Control voltage, (b) latch output, (c) reference level, and (d) amplifier output when global-gain control settling.

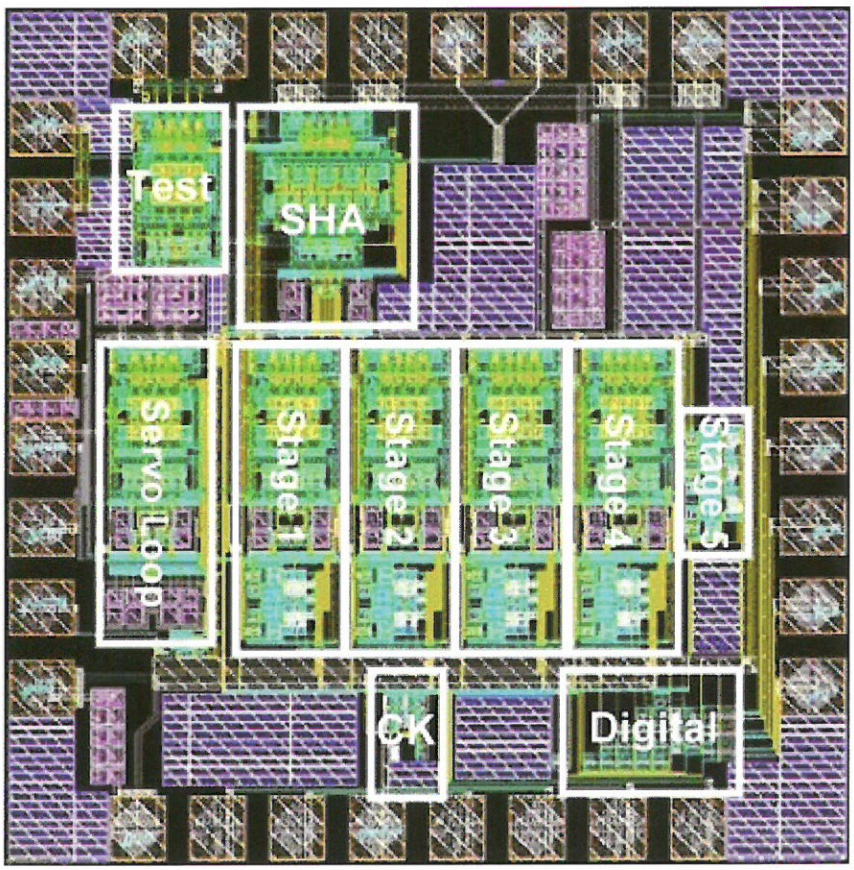


Figure 9. Layout of the ADC.

Designed with 0.18 μm CMOS technology, this ADC operates at the sampling rate of 160 MS/s at the supply voltage of 1.2 V for core circuit and 1.8 V for clocking. Fig. 9 shows the layout of the ADC. This chip occupies 1.04 x 1.05 mm^2 and the active area is 0.7 mm^2. Post-layout simulated results in Fig. 10 indicate that the maximum integral nonlinearity (INL) and differential nonlinearity (DNL) are 0.8 LSB and -0.92 LSB, respectively. The output spectrums are shown in Fig. 11. When input signal is at 19 MHz, the SNDR and SFDR are 35.6 dB and 40.5 dB. As input signal is near the Nyquist frequency, the SNDR and SFDR are 32.5 dB and 30.3 dB. Both ENOBs are above 5 bits. The performance specification of the proposed pipelined ADC is summarized in Table 1.

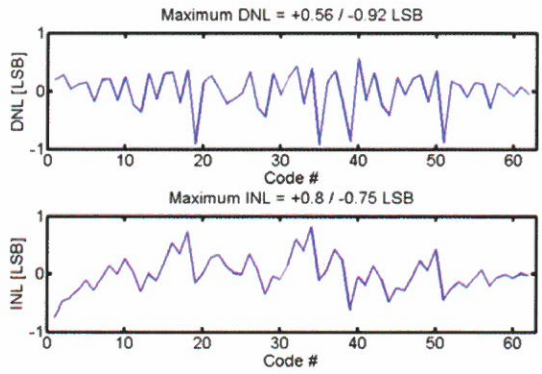
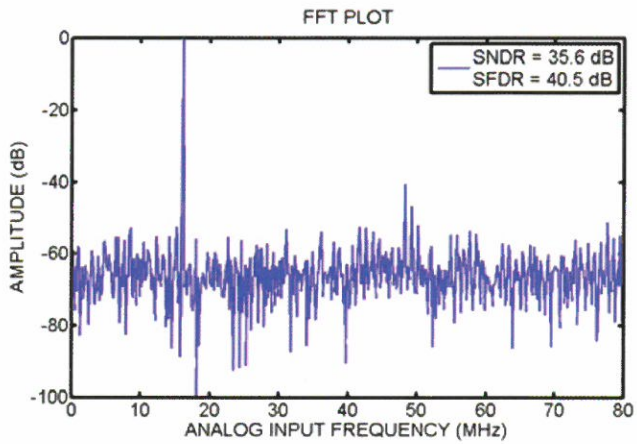
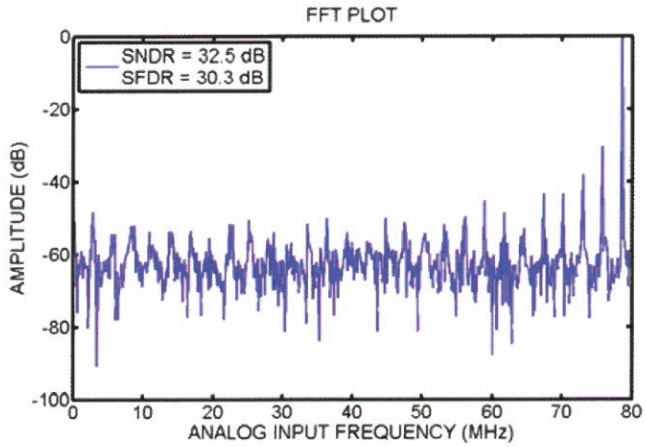


Figure 10. Simulated DNL and INL.



(a)



(b)

Figure 11. (a) FFT at F_{in} = 19 MHz, and (b) FFT at Fin near $F_S/2$.

Table 1. Performance Specification

Technology	CMOS 0.18 μm
Supply Voltage	1.2 V (Core) 1.8 V (Clocking)
Sampling Rate	160 MHz
Resolution	6-bit
Input Range	400 mV_{p-p}
Power Dissipation	90 mW
DNL/INL	0.5/0.4 LSB
SNDR@Fin=19 MHz @Fin=79MHz	35.6 dB 32.5 dB
SFDR@Fin=19 MHz @Fin=79MHz	40.5 dB 30.3 dB
Active Area	0.7 mm^2

4. Conclusion

This work designs the pipelined ADC with open-loop amplifiers without bias current sources. Replacing the resistors in amplifiers with the MOS transistors biased in triode region reduces the utilization of linear resistors. The low gain amplifier employs the transistors in triode region instead of the bias current source. The global-gain control loop utilizes a digital-like comparator to avoid bias current sources in the linear error amplifier. Consequently, no explicit bias circuit in the conventional amplifier is required in this pipelined ADC. Such bias-free techniques simplify the design complexity at modern high-speed pipelined A/D converter.

Acknowledgment

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一個採用開迴路放大器的無偏壓電路的六位元管線式類比數位轉換器

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輔仁大學電機工程學系

摘　要

本文提出一個六位元 160MS/s 採用開迴路放大器的無偏壓電路管線式類比數位轉換器。其放大器使用處於三極管區的 MOS 電晶體來代替電阻及電流源，以降低製程的變異與偏壓電路的需求。在放大器上使用全面性增益迴路來管理放大器的放大倍率，利用此迴路操作在低頻寬的特性，採用比較器作為誤差放大器，免除了線性放大器中所需要的電流源。此無偏壓電路類比數位轉換器採用 CMOS 0.18 μm 製程技術設計，其有效面積為 0.7mm^2。在核心電路採用 1.2V 的電壓源，而在時脈操作電路採用 1.8V 的電壓源，功率消耗為 90mW。電路佈局後的模擬顯示其 SNDR 與 SFDR 分別可達 35.6dB 及 40.5dB。最大的 INL 與 DNL 分別 0.85LSB 與 -0.92LSB。

關鍵字：管線式類比數位轉換器，開迴路放大器，增益控制，無偏壓電路。

光電式麥克生干涉儀之研製

張連璧* 潘沙婧 陳翰 張育彬
輔仁大學 物理系

摘 要

利用低廉、容易取得的光敏電晶體和史密特 TTL IC，分別做為光偵測器及波形整形器；此外結合自製的計數器，成功地研製出架構簡單、穩定且具有較佳抗雜訊能力及教學功能的光電式麥克生干涉儀。用此干涉儀測量氦氖雷射光波波長，其實驗誤差小於百分之一。

關鍵詞：麥克生干涉儀，光敏電晶體，干涉術 。

* Corresponding author, Tel.,+886-2-29052018; fax,+886-2-29021038
E-mail address: lbchang@mail.fju.edu.tw

緒 論

麥克生干涉儀最初是為了以太 (ether) 漂移實驗所精心設計的儀器 [1]，此儀器在近代物理學中占有非常重要地位的一個裝置，它為相對論提供了重要的實驗基礎。略加改變麥克生干涉儀可以設計成 Twyman-Green 干涉儀來檢測光學鏡片表面的平整度和缺陷及 Mach-Zehnder 干涉儀來檢測氣體折射率和密度變化 [2-4]。

麥克生干涉儀應用在大學光學教學實驗上可以做為量測光波波長及光的同調性等。早期是利用鈉原子放電管所激發出的 589.0nm 及 589.6 nm 黃光做為實驗的光源為主，其相干長度又稱同調長度 (coherence length) 約 1~2 公分，除了可以做為同心圓干涉條紋實驗的光源，測量光波波長，還可以安排測量光源的相干長度。由於實驗操作的困難度較高，以前大都安排在大三的光學實驗。

目前的光源大都是改以氦氖雷射所發出的 632.8 nm 的紅光為主，其相干長度可達數公尺之長，因此比起鈉原子放電管的黃光光源在操作同心圓干涉條紋實驗時容易許多，但缺點是：由於相干長度過長，因此要利用氦氖雷射所發出的紅光測量其相干長度，有實驗操作上的困難。目前大都只安排波長的測量。

然而目前教學型麥克生干涉儀大都屬於套件式的架構 [5]，其中一反射鏡和分光鏡都固定在一塊內含螺旋測微器，重量約 5 公斤重的基板上，以減少干涉條紋的晃動，而另一反射鏡移動的機構是利用槓桿的原理製作的。其原理敘述如下：螺旋測微器的頂端推動一個較長的槓桿臂，而該力臂的一端與一個圓柱轉軸相連，而轉軸的一端與一較短的槓桿臂相連，此槓桿臂用來推動反射鏡座。兩力臂的長度比為 1：20~25，依各儀器廠商的設計而定，因此轉動螺旋測微器 10μm 實際上鏡座只移動了 0.4~0.5μm，約半個波長的距離。此架構有不少缺點：

一、無法訓練學生如何架設干涉儀，並且掌握準直光線及對光的技巧。

二、機械部分過於精密、複雜，難以複製。

三、機械部分所累積的系統誤差過大，因此實驗誤差遠大於 1%。

除了利用機械槓桿來製作麥克生干涉儀之外，也有利用光電元件做為感測器的光電式麥克生干涉儀，但電路過於複雜，且抗雜訊能力較差 [6-7]。因此如何研製出一方面是個架構簡單、穩定、有較佳抗雜訊能力而且容易複製的干涉儀；另一方面它又可以降低系統誤差以提高實驗的精準度，同時又可以訓練學生基本的對光及準直光線技巧的麥克生干涉儀是本論文探討的重點。

我們以容易在一般電子材料行購買得到的價格低廉的光電元件並且能夠靈敏地偵測出氦氖雷射所發出的紅光其明暗變化做為本干涉儀的感測器。光敏電晶

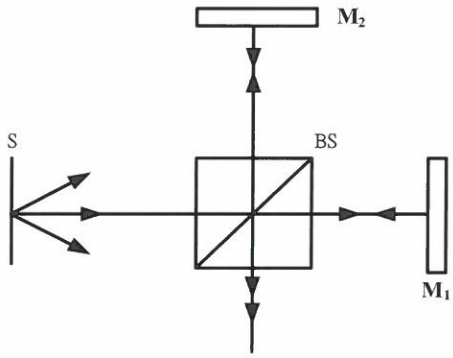
體 (phototransistor) 及光敏電阻 (photoresistor) 是最佳的候選元件而光敏二極體 (photodiode) 則被排出在外。這是因為前兩種光電元件都擁有極佳的光電流增益 (photocurrent gain) 而後者則無 [8-10]。若將對光強度變化的反應速度的因素考慮進去，實驗上我們發現光敏電晶體的反應速度為微秒級 (μs) 而光敏電阻的反應速度為毫秒級 (ms)。最後我們選擇了光敏電晶體做為自製麥克生干涉儀的光感測元件。另外，在計數電路與光感測電路之間增加了史密特觸發電路以消除因微弱震動而造成錯誤計數的問題，並提升計數的穩定性。

理論描述

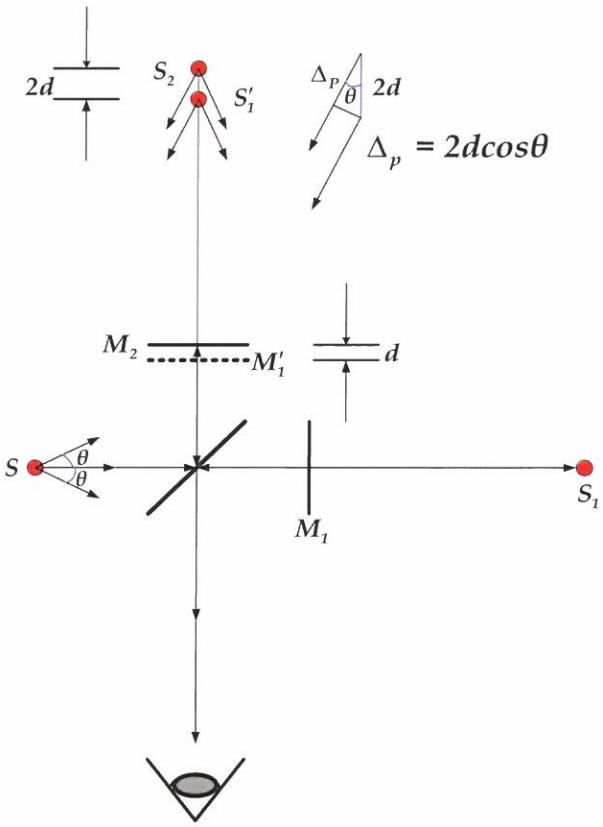
一般來說，麥克森干涉儀通常以單一波長的光源，透過分束鏡 (bean splitter) 裝置，製造出相同初始相位，且光強度相近的兩道光波進行疊加干涉，因此在觀測點 P 或光感應器的光強度可表示成 (1) 式：

(1)

其中 Δ_P 為由點光源 S 所發出之任一光線到光經分束鏡分成兩道光再經由兩面反射鏡 M_1 和 M_2 反射至分光鏡，然後相交於觀測點 P 之光程差，而 d 為 M_1 和 M_2 至分光鏡反射點的距離差，λ 為光波波長，θ 為此光線與中心線的夾角。圖一為麥克生干涉儀的簡圖，其中 BS 為立方體分束鏡，M_1 為移動式反射鏡，M_2 為固定式反射鏡。圖二為其等效光路圖。S_1、S_2 分別是光源 S 經由反射鏡 M_1 和 M_2 所成的鏡像而 M_1' 是反射鏡 M_1 經由分束鏡 BS 反射所成的鏡像。S_1' 是光源 S 經由反射鏡 M_1 與分束鏡 BS 連續兩次反射所成的虛像。其中 S_1' 和 S_2 間的距離為 2d。從觀察處所觀察到的干涉條紋可以看成是由兩個同調 (coherent) 點光源 S_1' 和 S_2 所發出的光波干涉所形成的。



圖一 麥克生干涉儀



圖二 等效光路

若 M_1' 平行於 M_2，則光程差 Δ_P 決定於光線入射的方向。假設光在分束器、M_1 及 M_2 的反射沒有造成額外的相位差，則等傾條紋的光程差為可表示成 (2) 式：

$$\Delta_P = 2d\cos\theta \tag{2}$$

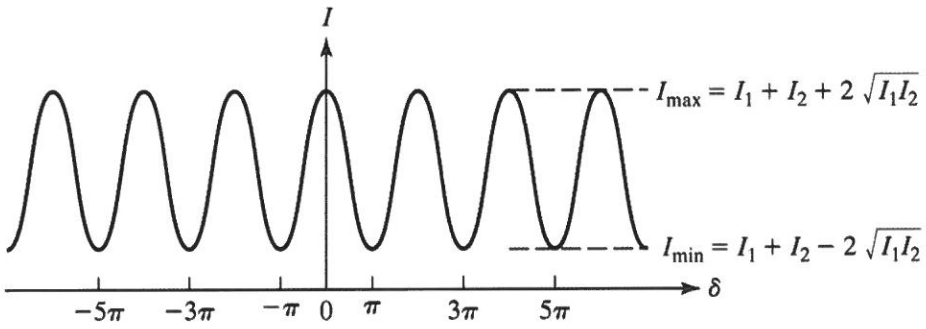
當 d 改變時，同心圓干涉條紋相對應的移動，不斷向中心縮陷或自中心湧出。光程差每改變一個波長時，消失或生出一條紋。在中心 $\theta = 0$，光程差為 2d，如果其為波長的整數倍，則同心圓條紋的中心為亮紋，反之如果 2d 為半波長的奇數倍，則同心圓明暗條紋的中心為暗紋。若以對應的相位 δ 來表示光程差 Δ_P，則二者的關係可表示成 (3) 式：

$$\delta = \frac{2\pi}{\lambda}\cdot\Delta_P \tag{3}$$

因此當光程差為波長的整數倍時，其所對應的相位是 2π 的整數倍，反之光程差為半波長的奇數倍時，相位是 π 的奇數倍。圖三顯示光強度 I 最大值發生在 δ 等於 2π 的整數倍（建設性干涉），而最小值發生在 π 的奇數倍（破壞性干涉），其結果可表示成 (4)、(5) 兩式：

$$I_{max} = I_1 + I_2 + 2\sqrt{I_1 I_2} \tag{4}$$

$$I_{min} = I_1 + I_2 - 2\sqrt{I_1 I_2} \tag{5}$$



圖三 干涉條紋強度隨相位 變化

當兩道光的強度越接近時，I_{min} 越接近零，則明暗對比也就越好，這一點對於利用史密特觸發電路將圖三的波型整形成方波波型非常重要。因此干涉條紋的對比值 (visibility) V 可以定義如下：

$$V = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \tag{6}$$

如果 I_1、I_2 相同且皆等於 I_0，則 (1) 式可表示成 (7) 式：

$$I_P = 4I_0 \cos^2(\frac{\delta}{2}) \tag{7}$$

當移動 M_1 反射鏡時，同心圓干涉條紋中心會產生明暗變化，經由史密特觸發電路所轉換的方波就會觸發計數器，因而可以正確地記錄亮紋或暗紋的變化次數，其變化次數 N 與 M_1 移動的距離 Δd 可表示成 (8) 式：

$$2\Delta d = N\lambda \tag{8}$$

變化次數 N 可由 (8) 式得出：

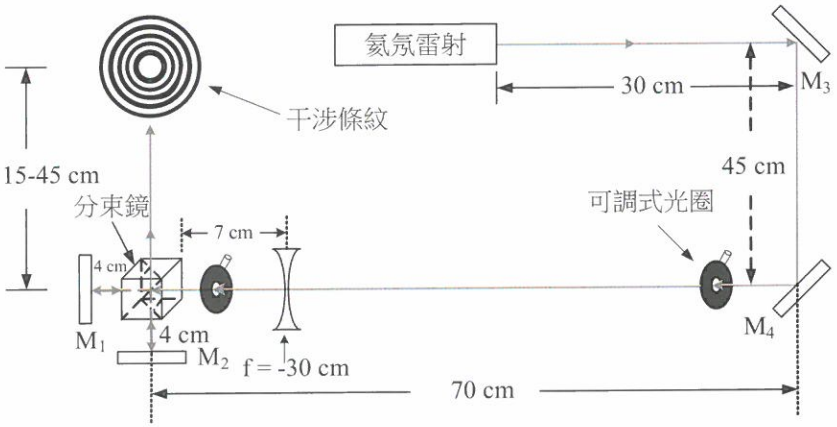
$$N = \frac{2\Delta d}{\lambda} \tag{9}$$

當 $\lambda = 0.6328\mu m$ 時，轉動螺旋測微器一圈時，其移動的距離為 500 微米 (μm)，則亮紋或暗紋的變化次數為 1000/0.6328 等於 1580.278。

實驗架構

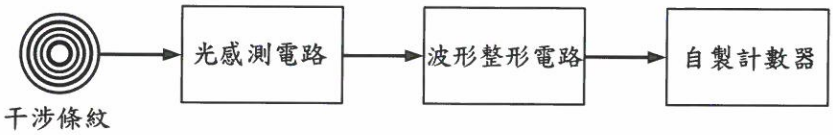
整台光電式麥克生干涉儀可以分成光路和電路兩部分。光路部分見圖四。光源是一台 5 mW 的氦氖雷射 (Melles Griot 25-LHP-111-249)，目前只剩約 3.5 mW。光由雷射射出，經兩片鍍鋁的 M_3 和 M_4 反射鏡入射至一發散透鏡，然後經由分束鏡將光分成兩道，分別入射至同樣是鍍鋁的 M_1 和 M_2 反射鏡，其中 M_1 架在移動平台上可移動而 M_2 固定不動。當這兩道光反射後經由分束鏡後，合而為一形成同心圓的明暗干涉條紋。光路上的兩個光圈 (Iris) 是用來對光及準直光線，當鏡面不慎觸碰到導致干涉條紋偏掉或消失時，可以藉由這兩個光圈重新

準直。相關的間距請參考圖四。光感應元件至分束鏡反射中心的距離從 15 cm 到 40 cm，因此該元件可放的位置範圍相當的寬。干涉儀必須架設在具有防震功能的光學桌上。

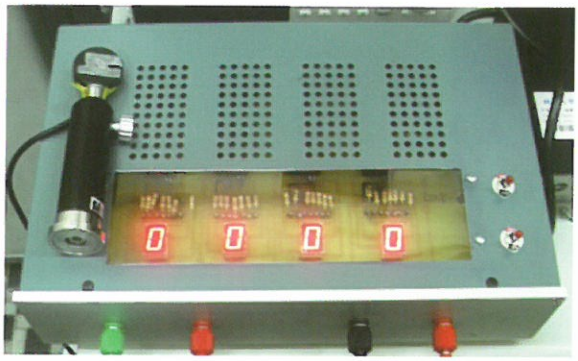


圖四 光電式麥克生干涉儀之光路圖

電路部分請參考圖五的方塊示意圖。干涉條紋中心的明暗變化由光感應電路負責偵測，光偵測元件為一顆 NPN 的光敏電晶體 (型號 LPT055，聯宇電子)，其反應最敏感的波長為 900 nm，上升與下降時間分別為 10μs 及 15μs。光敏電晶體之集極 (collector) 接至 5 伏特 的直流電壓源，而射極 (emitter) 串聯一顆 910Ω的電阻器，電阻器的另一端接地，電壓訊號由射極端輸出至波型整形電路，而該電路由一顆 7414 TTL IC —史密特觸發反相器所構成，其上轉折電壓 (the upper trip point) 或正向臨界電壓 (the positive going threshold voltage) 約 1.6 V，而下轉折電壓 (the lower trip point) 或負向臨界電壓 (the negative going threshold voltage) 約 0.8 V，因此磁滯區 (hysteresis) 約為 0.8 V。史密特觸發器因具有磁滯區而可以大大降低因雜訊干擾而造成的錯誤觸發，並將圖三之波型轉換成方波，而方波的高電位約 4.8 V，低電位約 0.2 V。史密特觸發器的輸出端接至自製的計數器 (見圖六) 做為觸發源。該計數器由四組相同的十進位計數電路所組成。每一組計數電路由一顆 7490 TTL IC —非同步十進位計數器，用來記錄干涉條紋明暗變化的次數，接著串連一顆 7475 TTL IC —四個位元栓鎖器，用來暫存 7490 所記錄的二進位數字，再串接一顆 7447 TTL IC —共陽極 BCD (十進制) 轉七段顯示解碼器，用來將 7475 所暫存的二進位數字解碼及驅動七段顯示 LED。最後串接一顆共陽極七段顯示 LED，用來顯示 0~9 的十進位數字。



圖五 電路方塊示意圖



圖六 自製的十進位計數器

由於轉動螺旋測微器一圈時，亮紋或暗紋的變化次數約為 1580，轉動一圈平均時間約 1 秒，因此亮紋或暗紋的變化一次的時間少於 1 毫秒，所以在光感應元件的反應時間必須遠小於 1 毫秒。

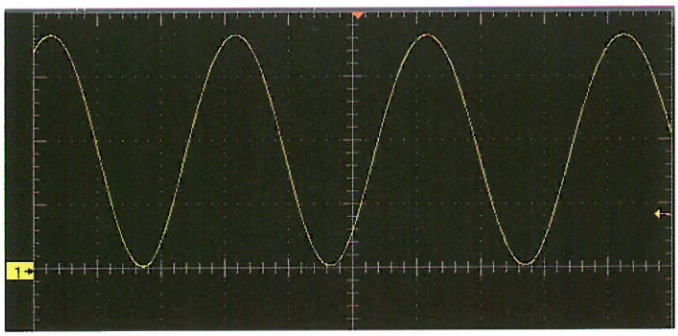
實驗結果與討論

3.5 mW 的雷射光經過整個光路最後由 M_1 和 M_2 反射至光敏電晶體的功率 P_1 和 P_2 分別為 0.484 mW 及 0.522 mW，其比值約為 0.93，所對應的 I_{max} 和 I_{min} 分別為 3.86 和 0.00127，因此干涉條紋的明暗對比值 V 為 0.999 極接近理想值 1。

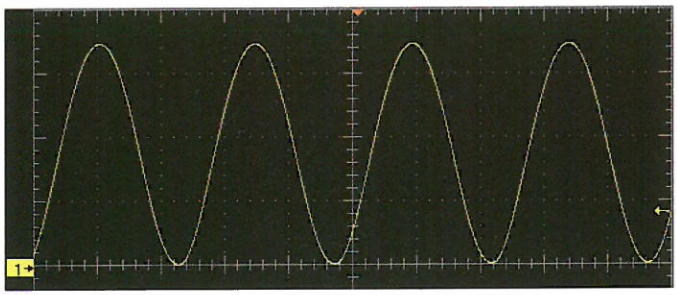
圖七 (a) 至圖七 (c) 為光敏電晶體至分束鏡反射中心的距離分別 15 cm、25 cm 和 40 cm 時之干涉條紋強度（已轉換成電壓值）對光程差之變化圖。圖中垂

直刻度每一大格皆為 1 V，其中最大電壓分別為 3.66 V、3.51 V 及 2.58 V，而最小電壓分別為 60 mV、40 mV 及 40 mV。由於光的強度會隨距離增加而減弱，因此最大電壓會隨距離遞減；另外，如果同心圓中心的面積沒有完全涵蓋光感測頭，就會有少許外圍的光進入感測頭，或則是由於 I_1、I_2 不完全相等，當破壞性干涉發生時，不會完全抵銷，因此最小電壓不會完全為零。

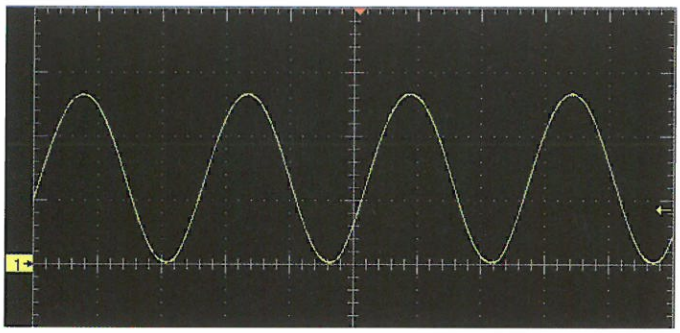
由於最大的電壓值皆遠大於正向臨界電壓約 1.6 V，而最小值皆小於負向臨界電壓約 0.8 V (或 800 mV)，所以能夠正常的轉換成方波訊號。除此之外，圖中的波形像極了 (7) 式的函數圖形，這是由於 I_1、I_2 相當接近。



圖七 (a) 離分束鏡心 15 cm 處光強度之變化

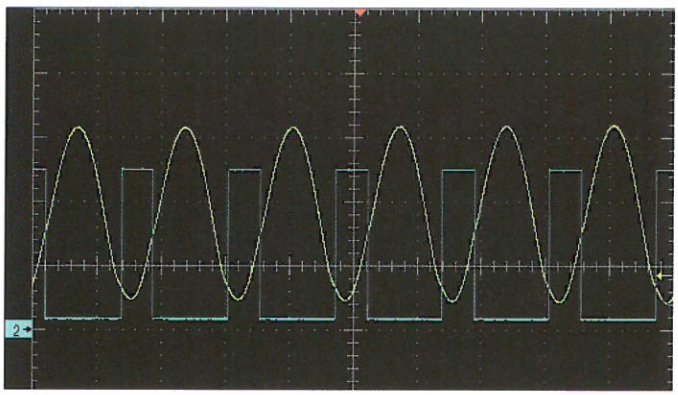


圖七 (b) 離分束鏡心 25 cm 處光強度之變化

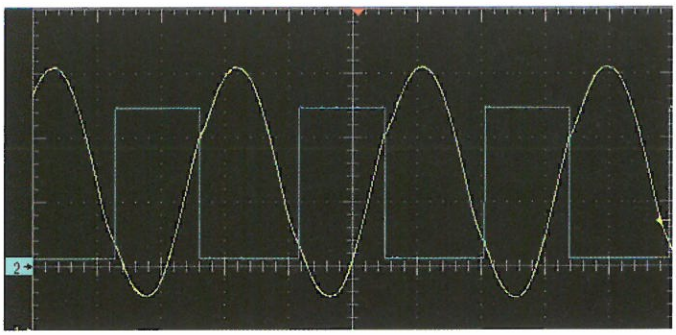


圖七 (c) 離分束鏡心 40 cm 處光強度之變化

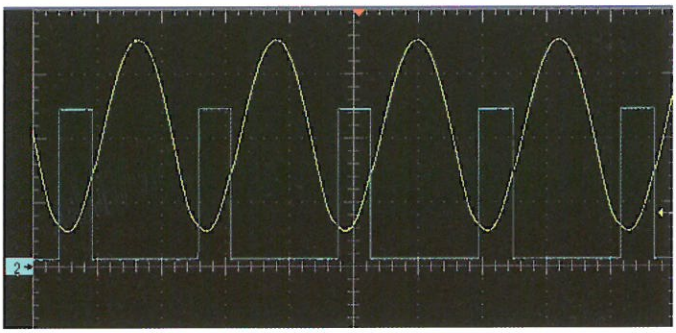
圖八 (a) 至圖八 (c) 是感測電路輸出端接至史密特觸發反相器後同時記錄原感測波形及轉後的方波波形。由於光感測電路的輸出阻抗準位與波形整形電路的輸入阻抗準位並不匹配，因而造成原始訊號的電壓準位的改變，尤其是最小值由數十毫伏提高至數百毫伏，同時由於史密特觸發反相器的基本電路架構是個正回授的比較器，因此在轉換成方波的過程中，由低準位 (約 0.2 V) 轉變成高準位 (約 4.8 V) 或高準位轉變成低準位時由於瞬間電壓變化過大，在史密特觸發反相器的電壓觸發點 0.8 V 和 1.6V 的地方，原始訊號發生了波形的失真 distortion)。



圖八 (a) 15 cm 處光強度之變化及轉換後之方波波形



圖八 (b) 25 cm 處光強度之變化及轉換後之方波波形



圖八 (c) 40 cm 處光強度之變化及轉換後之方波波形

圖七和圖八是左右快速轉動螺旋測微器造成光程差的變化，因而產生干涉條紋明暗變化的結果。

移動 M_1 的線性平台與螺旋測微器分別為 Newport M-460A-X 及 SM13，而其最小增量為 1μm。表一 (a) 至表一 (c) 代表當轉動螺旋測微器一圈；即移動 M_1 500μm (精確度為 0.2%)，光敏電晶體在離分束鏡心 15 cm、25 cm 及 40 cm 處所測得條紋明暗變化次數。實驗過程中我們任意挑選四顆電晶體並將其編號成 1—4 號，如表一所示，以確認實驗的精準度與特定的光敏電晶體無關，而且每顆重複三次相同的實驗操作，結果發現當光敏電晶體置於 25 cm 處，實驗誤差最小，其次為 40 cm 處，而置於 15 cm 處的實驗誤差最大。原因可能是：於 25 cm 處，同心圓中心的面積較 15 cm 處的面積大，而且干涉光的強度適中，然而於 15 cm 處，最內圈的面積最小，容易受到鄰近干涉環的影響，因而造成額外的誤差。所有的實驗誤差皆小於百分之一。整體實驗的平均誤差為 0.36%。

此外我們又對系統做了約三小時穩定性測試。結果數字維持不變，這表示在測量時，數字的變化源自於條紋明暗的變化而非周遭環境的變化所造成的。因此誤差來主要自於系統誤差：螺旋測微器 (0.2%)，及人為操作誤差所致。

表一 (a) 離分束鏡心 15 cm 處，移動 M_1 500 μm 所測到的條紋變化次數

元件編號	距離	測量順序	明暗變化次數	平均值	誤差
1	15 cm	1	1587	1587.7	0.49%
		2	1571		
		3	1605		
2	15 cm	1	1590	1588	0.53%
		2	1588		
		3	1587		
3	15 cm	1	1575	1584	0.23%
		2	1590		
		3	1586		
4	15 cm	1	1585	1590	0.63%
		2	1593		
		3	1592		

表一 (b) 離分束鏡心 25 cm 處，移動 M_1 500 μm 所測到的條紋變化次數

元件編號	距離	測量順序	明暗變化次數	平均值	誤差
1	25 cm	1	1576	1584.7	0.30%
		2	1589		
		3	1589		
2	25 cm	1	1584	1582.7	0.17%
		2	1588		
		3	1576		
3	25 cm	1	1583	1583	0.19%
		2	1585		
		3	1581		
4	25 cm	1	1586	1586.7	0.42%
		2	1581		
		3	1593		

表一 (c) 離分束鏡心 40 cm 處，移動 M_1 500 μm 所測到的條紋變化次數

元件編號	距離	測量順序	明暗變化次數	平均值	誤差
1	40 cm	1	1583	1587.7	0.49%
		2	1592		
		3	1588		
2	40 cm	1	1586	1586.3	0.40%
		2	1586		
		3	1587		
3	40 cm	1	1591	1587	0.44%
		2	1586		
		3	1584		
4	40 cm	1	1583	1581.3	0.084%
		2	1574		
		3	1587		

結　論

本篇論文描述了整個光電式麥克生干涉儀研製的細節、及實驗的結果，成功地結合了光學與電子學的知識與技術，完成了干涉儀的研製。本干涉儀的光電元件容易取得且電路簡易，容易複製。另一個優點就是光感測器可置放相當大的範圍 (25cm)，而且在這個範圍內，實驗誤差皆在百分之一以內，這與機械槓桿式的干涉儀相比，足足提升了一個數量級。除此之外；還可以讓學生學會對光、調整光路的技巧，並且學習測量光電訊號及如何正確判讀。

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The study and implementation of a photonic Michelson interferometer

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Abstract

Using a low-cost and commercially available phototransistor and Schmitt trigger with immunity to false triggering as the light sensor and the waveform converter respectively, as well as a homemade counter, we successfully designed and constructed a simple reliable photonic Michelson interferometer for an undergraduate optics laboratory. The results of experiments for measuring the wavelength of red helium-neon laser light achieve better than 1% accuracy.

Key words: Michelson interferometer, phototransistor, interferometry

利用 RED 機制在非結構化的 P2P 網路中改善負載平衡問題

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摘　要

Peer-to-peer (P2P) 的技術與其所架構出來的網路是現今的網路熱門應用之一。現實生活中 P2P 網路大多是以非結構化的形式來呈現，在這樣的網路中，節點要得到想要的檔案通常是藉由廣播給所有的鄰居來進行搜尋，卻因此造成多數節點有著極大的負擔。若有某些節點處在較熱門的路徑上，也會因為往來的訊息量相對較多，造成該節點的負載比其他節點高。本篇論文提出一個檔案搜尋的轉送機制，利用 Random Early Detection (RED) 來判斷是否要轉送收到的 Search_Reply，使得節點的負載能得到改善而不至於負載過重。

實驗數據顯示，我們的方法可以減少產生 20% 的訊息量，使得網路負載降低。所挑選路徑之負載僅為沒使用 RED 的方法之 30% 左右，代表我們的方法能降低負載過高之節點的壓力，使得網路中的節點負載標準差相對較低，達到改善網路中節點負載的效果。

關鍵詞：負載平衡、非結構化點對點系統、隨機早期偵測

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1. 前 言

Peer-to-peer（簡稱 P2P）技術 [1-5] 是近年來網路上熱門的技術之一。P2P 系統的架構 [6-8] 可以分成非結構化（Unstructured）和結構化（Structured）兩種。在非結構化 P2P 網路中，既沒有集中式的目錄伺服器，也無法對網路拓樸和資料分佈做精確的控制。若有節點欲發出搜尋請求，則通常必須對所有鄰居做廣播的動作。若此網路有 N 個節點，則要找到所需的檔案複雜度為 O(N)。而結構化 P2P 網路，則是所分享的檔案分佈以及該網路拓樸的特性都藉由分散式雜湊表（Distributed Hash Table, DHT）做緊密的控制。在這樣的網路中，每個節點會被分配到一個 ID，每個檔案也會經由雜湊函數被分配到一個 ID。當有節點要搜尋某檔案，它會先藉由雜湊函數得出此檔案之 ID，再將請求訊息傳至目前負責保管此檔案 ID 之節點。若網路中有 N 個節點，則要找到所需的檔案複雜度僅為 O(logN)。雖然在具結構化的 P2P 網路中搜尋檔案的效能較佳、發送請求的總訊息數較非結構化的 P2P 網路少，但由於結構化的 P2P 網路需要花較多成本在維護整個系統，而且上線下線頻繁會使得效能下降，因此實際生活中大多為非結構化的 P2P 網路。

本篇論文的研究重點是在非結構化的 P2P 網路中，改善節點廣播過多的請求問題以及節點的負載平衡問題，使得網路不至於壅塞、節點不至於負載過重。首先要改善的部分是在一般的情況中，當節點發送請求時往往都是使用廣播的方式，此時對於在廣播路徑中的節點而言會造成負擔，因為相同的請求可能會因為路徑不同而在某段時間內不斷的被轉送或經過同一個節點。因此該節點在轉送檔案搜尋訊息時，若是全部轉送，則一段時間之後可能會有許多的檔案下載路徑會經過該節點，造成負載過重，拉長檔案下載所需時間。所以該節點若能利用某種機制來決定對一部分的檔案搜尋相關訊息不要加以轉送，可以降低該節點本身以及往後路徑中的節點的負載，進而使得網路中的節點負載平均。當節點所在位置處於熱門路徑上，該使用何種機制來使得訊息減少經過該節點，以減緩或降低不斷加重的負載。我們提議在節點中使用 Random Early Detection（RED）[9]的概念，來判斷是否轉送檔案搜尋相關訊息。當負載上升時，利用 RED 提早將一部分搜尋訊息丟棄，可以避免該節點的負載快速上升，使得負載能導入其他路徑，讓整體負載分布較為平衡。

本篇論文其餘部分結構如下：在第二節中，我們將介紹既有的改善負載平衡的方式與相關研究，第三節則是詳細介紹我們的系統概述，以及所提出之方法。第四節是實驗數據及分析結果，而第五節則為此論文之結論。

2. 相關研究

在降低負載與改善負載平衡方面，有一類方法是藉由減少廣播出去的總查詢訊息數，以減少整體流量並降低節點負擔 [10][11]。[10] 所使用的方法是利用先在網路的外圍找尋一些節點作為 Corner stone，將節點的檔案搜尋訊息複製給這些 Corner stone，再由這些 Corner stone 同時由外向內進行廣播檔案搜尋訊息的動作。如此可以有效減少多餘的查詢訊息被廣播出去，並且加快找到所需檔案的所在位置。[11] 則是在廣播檔案搜尋的訊息時，只將訊息發給 K 個鄰居，這 K 個鄰居接著只轉送給它的一個鄰居，直到找到檔案或 Time-to-Live 值降至零為止。此方法能有效降低節點負載，但難以決定出一個適當的 K 值。

將檔案複製給鄰居，藉此分散流量以降低節點負載，也可提升負載平衡 [12-14]。[13] 的方法是先找出負載大於整體網路平均值的節點，這些節點會將收到的請求訊息以及所需檔案轉送給備份節點 (鄰居或其他負載較輕的節點)。[14] 的方法則是利用熱擴散的概念，檔案存取比例高的節點會將檔案複製給存取比例低的鄰居，如熱往外擴散一般，以拉近所有節點的存取比例。此類方法必須藉由節點間彼此交換訊息，才能得出整體負載平均值。若網路中的節點個數眾多，則會產生大量的訊息。

還有一類方法是改善熱門路徑中節點負載過重的問題。當所有可能的檔案下載路徑皆為負載過重時，可以找出最短路徑上負載最重的節點，將其負載重新分配給鄰居 [15]。或者是當某一節點負載過重，則找出傳送訊息過來最多的鄰居，強制要求其將訊息改導向其他負載較輕的鄰居節點 [16]。不過若是負載過重的原因是節點本身處於熱門路徑上，或是節點擁有熱門檔案，則運用此方法將無法得到明顯的改善，仍須搭配檔案複製。

3. 利用 RED 之負載平衡機制

3.1 系統概述

我們假設一個非結構化的網路拓樸，每個節點會有數個鄰居。在此網路中，當一個節點（稱為起始節點）想要取得某個檔案時，它會執行以下步驟（如圖 1）：起始節點先對數個鄰居發送 Search_Request 訊息，收到此訊息的節點會繼續轉送給鄰居。

當擁有此檔案的節點（稱為目的節點）收到 Search_Request 後，會發送 Search_Reply 訊息並按照原路徑回傳給起始節點。起始節點再挑選某路徑發送 Transmit_Request 給目的節點來要求檔案，最後目的節點將檔案依路徑傳回。

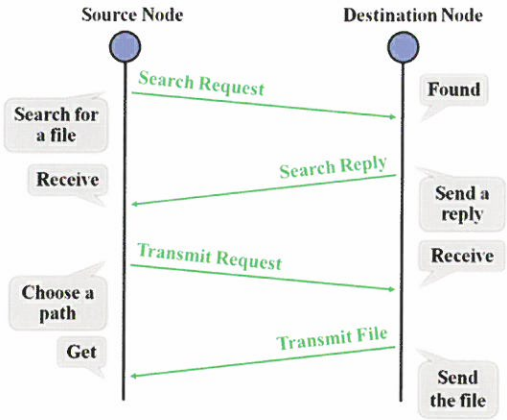

圖 1 檔案傳輸流程圖

當節點收到 Search_Reply 的訊息，代表著這條路徑中已經有節點搜尋到起始節點所需要的檔案。若將此訊息轉送回起始節點，表示此節點將有可能再次收到來自同樣請求的 Transmit_Request 與最終的檔案傳輸。所以若節點的負載高又允許訊息通過，將可能讓節點的負載在往後的時間中變得更加嚴重。所以我們試著將 RED 的機制運用在此。當節點的負載高時則中止轉送此訊息，起始節點就不可能挑選此路徑做檔案傳輸，如此便能減少此節點的負擔。所以節點會在收到 Search_Reply 時，使用 RED 的機制來決定是否要將該 Search_Reply 繼續轉送。

3.2 在非結構性點對點網路中使用 RED

我們提出一個 Random Early Detection in Unstructured P2P Networks（簡稱 REDUP2P）的方法，該方法包含下列步驟：

Step1: 節點在網路初始化以及獲得新檔案時，會將節點本身所擁有檔案數量告知所有鄰居，其鄰居再將所蒐集到的資訊儲存起來以便於 Step2 使用，如圖 2 所示。

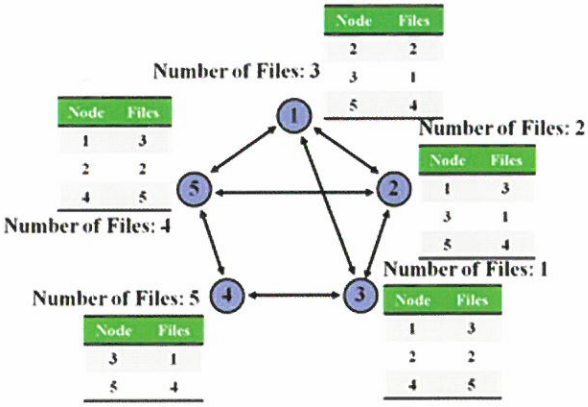

圖 2 網路中的節點會彼此告知所擁有的檔案數量

Step2: 起始節點會對半數的鄰居發出 Search_Request 訊息。首先，從節點本身所儲存鄰居檔案數量的表格中挑選檔案數量前 1/4 多的節點，再來於剩下未挑選的鄰居節點中隨機挑選 1/3。如此的原因則是考量到若全部 P2P 網路中的節點都只挑選檔案數量多的鄰居，會導致流量往檔案數量多的節點集中，造成這些節點負擔過重，故我們的挑選方式可以達到分流效果。

Step3: 當節點有所需之檔案時，則會發送 Search_Reply 訊息來通知起始節點。當某中間節點收到 Search_Reply 訊息時，會使用 RED 機制來判斷是否要繼續轉送。當該節點的負載狀況為低於某一門檻 α_1 則會讓 Search_Reply 訊息通過；若介於門檻值 α_1 和 α_2 之間，則按比例中止 Search_Reply 訊息的轉送動作；但若負載程度高於門檻 α_2 則會完全中止 Search_Reply 訊息的轉送動作，如圖 3 所示。在 Search_Reply 訊息中記錄著所經過的完整路徑，以及此路徑中的最高負載值。倘若該中間節點決定繼續轉送此 Search_Reply，則判斷該節點負載是否高於此訊息中所記錄的負載值，若是則將該節點的負載值覆蓋至訊息中，然後繼續將 Search_Reply 訊息轉送給路徑中的下一個節點。

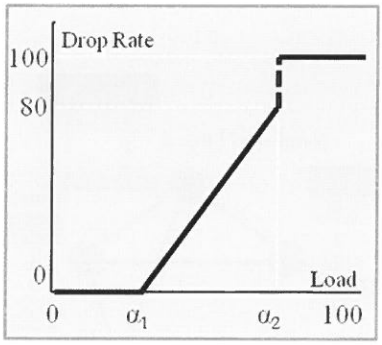

圖 3 節點負載與訊息中止機率關係圖

Step4: 起始節點可能會收到一至數個 Search_Reply 訊息，它會從中挑選一個較早抵達且負載值低於 β 的 Search_Reply 訊息，針對其路徑發送 Transmit_Request 來要求檔案。若檔案遲遲沒有回傳造成 Time Out，則起始節點會從收到的 Search_Reply 訊息中挑選一個未挑選過且所紀錄的路徑負載值最低，來當作下一次發送的 Transmit_Request 訊息，若連續 X 次 Time Out 則宣告此次搜尋失敗。當目的節點收到 Transmit_Request 訊息時，會直接將檔案依原路徑傳回。

4. 效能評估

4.1 模擬環境

我們撰寫一個 JAVA 模擬程式來進行效能評估，實驗參數如下：我們假設網路中共有 500 個節點，每個節點的頻寬為 75~125 個單位頻寬。每個節點平均有五個相鄰節點，採隨機方式與其它節點互連。在網路中有 500 種不同檔案，每種檔案各有 25 個副本，採隨機分布於網路的節點之中。在發送 Search_Request 訊息時，我們設定 TTL 為 8。傳送一個控制訊息會消耗一個單位頻寬，而檔案會分成十個片段，每個片段在傳輸時會消耗十個單位頻寬。在我們的方法中，設定有兩個負載門檻分別是 $\alpha 1$、$\alpha 2$，在此我們將此二值設為 50% 與 90%。當節點在收到 Search_Reply 訊息時，若負載介於此二值之間則會有訊息中止轉送的可能會出現，機率從 0% 成正比至 80%。

在實驗當中，我們會將我們的方法和其他三種方法做比較：第一種稱為 Threshold@SR，就是當節點在收到 Search_Reply 訊息時，若其負載高於 90% 則中止

該訊息轉送。第二種稱為 Threshold@TR，是當節點在收到 Transmit_Request 訊息時，若負載高於 90% 則中止該訊息轉送。第三個是 NoRED，此方法是轉送所有訊息，不會考量負載高低。

4.2 模擬結果

圖 4 和圖 5 分別畫出四個方法產生的訊息量以及網路平均負載。我們可以看到 REDUP2P 所產生的訊息量及網路負載為最少，NoRED 最多，而 Threshold@SR 與 Threshold@TR 則是略多於 REDUP2P。這是因為 REDUP2P 在節點收到 Search_Reply 訊息的階段有做負載控制，若節點負載高於 50% 則開始隨著節點負載而增加中止訊息轉送的機率，因此產生的訊息量及網路負載就會變得較低。

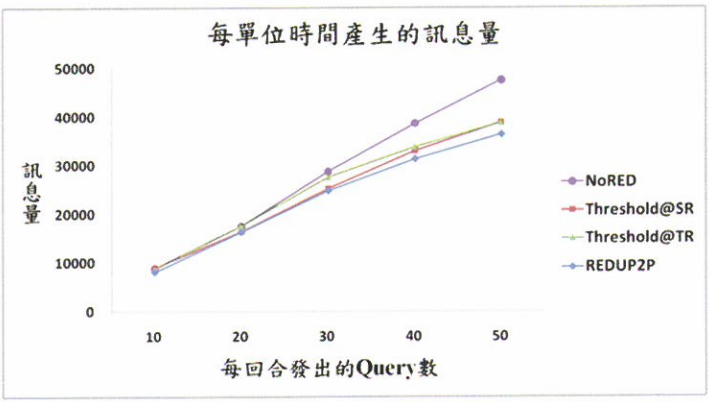

圖 4 每單位時間產生的訊息量

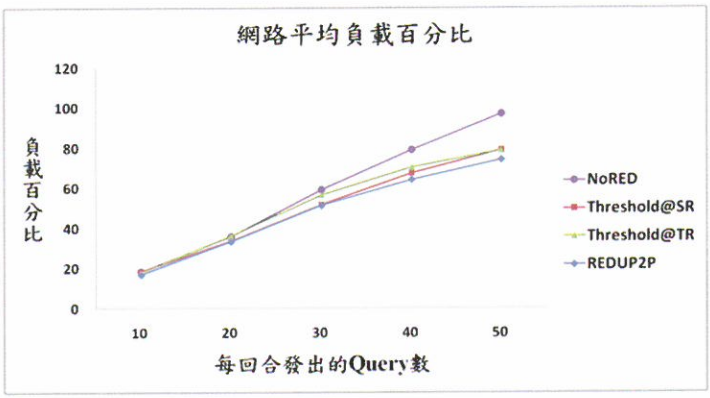

圖 5 網路平均負載百分比

圖 6 和圖 7 分別顯示四個方法所挑選路徑之最高負載，以及節點負載之標準差。REDUP2P 因為是在節點於收到 Search_Reply 訊息時做負載控制，如此可避免起始節點挑選到負載過重之路徑，造成路徑中的節點負載變得更重。Threshold@SR 和 Threshold@TR 都僅使用單一 threshold 來判斷是否轉送訊息，所挑選路徑之負載會比 REDUP2P 較高。NoRED 則是最高。節點負載標準差也是有著同樣的順序，顯示我們的 REDUP2P 確實能讓所有節點的負載能較為平均。

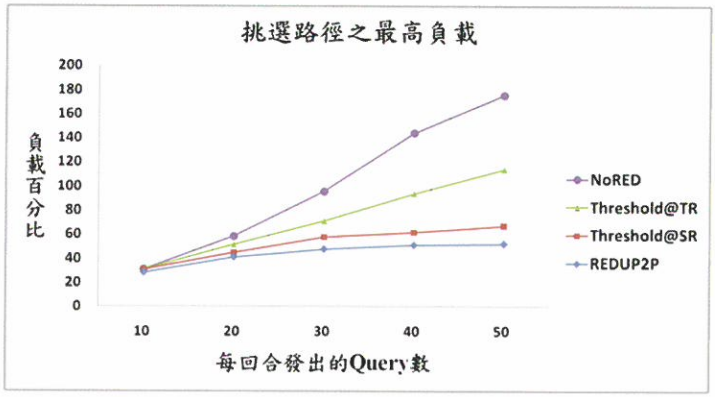

圖 6 挑選路徑之最高負載

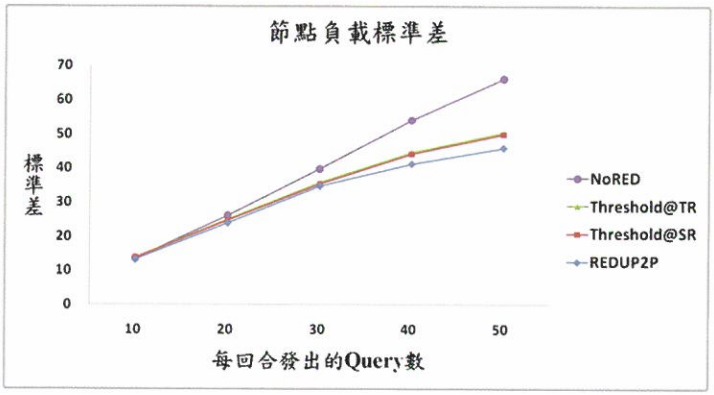

圖 7 節點負載標準差

圖 8 列出檔案下載所需時間，REDUP2P 方法在所需要的時間裡總是相對最低，這是因為我們有做負載控制使得所挑選的路徑其路徑上的節點負載都不致於太高，所以可以較快的速度從檔案搜尋進入到檔案下載的動作。最耗時的是 Threshold@TR，此方法在檔案下載的所需時間和其他三個方法相比相差很大。因為此方法將負載控管設於節點收到 Transmit_Request 訊息時，導致有可能所發出之 Transmit_Request 訊息被中間節點拋棄。而必須挑選另一路徑重新發送 Transmit_Request，導致下載檔案所需時間最高。

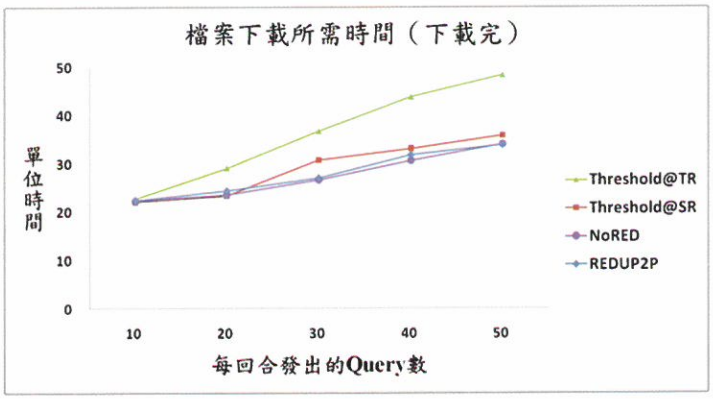

圖 8 檔案下載完成所需時間

5. 結　論

在非結構化的 P2P 網路中，若使用廣播的搜尋方式，可以有較高的檔案搜尋成功率，但是卻會造成節點負載過高。我們採用半廣播的方式，搭配有方向性的引導節點來轉送訊息。再利用 RED 機制作用於 Search_Reply，使得網路中的節點能有較好的負載平衡效果。實驗結果顯示，我們的方法產生的訊息量為相對最低，因此網路整體的負載也相對最低，節點的負載標準差為四個方法之中相對最低，代表我們的方法能讓網路中的節點有著較為均衡的負載。

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Using Random Early Detection to Improve Load Balancing in Unstructured P2P Networks

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Abstract

The architecture of the network system formed by Peer-to-peer (P2P) technology is one of the most popular applications on today's Internet. However, most P2P networks currently in use operate in an unstructured style. The query broadcast employed by the peers to search for a file often results in great burdens on the network. Furthermore, for those nodes located on popular paths, they will receive more messages and thus have higher loads than the others. In this work, we propose a message processing and forwarding mechanism which does not lead to overloads on the nodes in an unstructured P2P network. When a node searches for a file, it would use our mechanism to choose which neighbors to send a Search_Request. When a node receives a Search_Reply message, it would decide whether to forward the message or not using the Random Early Detection (RED) scheme on its own load level. Simulation result shows that our method can reduce the number of messages by twenty percent and the average load on the file transmission path by seventy percent, respectively, compared to when RED is not used. This shows that our method can achieve load balancing among the nodes in the network.

Key words: Load Balancing, Unstructured P2P, Random Early Detection

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高電容多孔性氧化釕氫離子感測器之研製

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摘　要

本研究係以電化學沉積之循環伏安法 (Cyclic Voltammetry) 備製高電容多孔性 (Porous) 的氧化釕 (Ruthenium Oxide, RuO_2) 薄膜，作為感測器之工作電極，此備製方法具快速與成本低廉之優點。氧化釕薄膜具有高導電度、高表面積及較佳之電化學可逆性，且於酸性水溶液中具高穩定性與良好電催化特性。故藉由氧化釕薄膜表面結構，可增加薄膜之多孔特性及電極表面積，有效提升氧化釕薄膜與待測溶液間之接觸面積，以實現最佳線性度、感測度與穩定度之工作電極，並進一步將其應用於氫離子感測。

關鍵詞：循環伏安法、高電容、多孔性、氧化釕、氫離子。

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1. 前　言

於 1971 年 Trasatti 與 Buzznaca 等人 [1, 2] 發現以熱分解 (Thermal Decomposition) 之循環伏安法 (Cyclic Voltammetry, CV) 所製備之二氧化釕電極，其電位範圍介於－ 0.2 V 至 1.4 V 呈現方形行為，此方形之循環伏安行為非常適合作為電容材料。於 1975 年 Conway 等人 [3] 以循環伏安法將釕金屬直接轉變成氧化釕，發現具良好之可逆性及穩定性。於 1995 年，Zheng 等人 [4] 以溶膠 - 凝膠法 (Sol-Gel) 備製含水二氧化釕，其電容值可達 720 F/g。於 2007 年，Gujar 等人 [5] 以電化學法備製氧化釕薄膜，其電容值係 498 F/g。

本研究選擇氧化釕 (Ruthenium Oxides, RuO_2) 薄膜為主要研究方向，因釕 (Ruthenium, Ru) 係一種貴重金屬材料，其氧化物具有超高電容量之儲電效果，氧化釕具有如金屬般之低電阻係數 (小於 10^{-4} ohm-cm) 及高比表面積 (約 800-1000 cm^2/g) 的特性，由文獻 [6-9] 得知以氧化釕作為離子感測元件具有諸多優點，例如高導電度、高表面積及酵素附著性佳等。

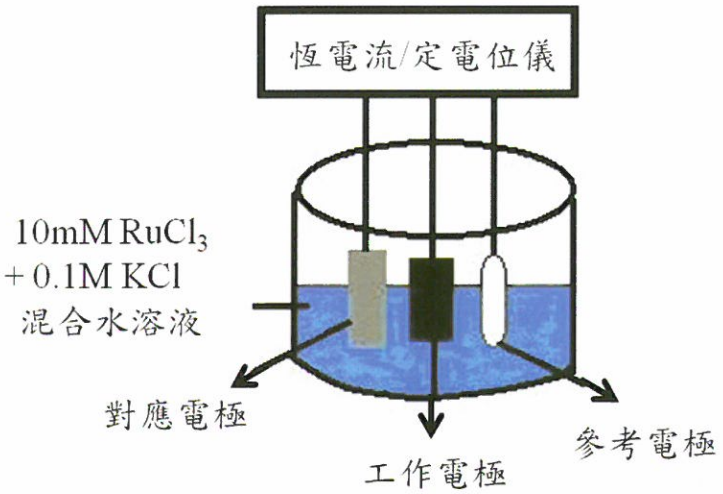
電化學沉積法之循環伏安法備製氧化釕薄膜具製程簡便、快速及成本低等優點，且最大特色係可控制薄膜之沉積型態。故本研究係利用循環伏安法備製氧化釕薄膜感測元件，分析氧化釕薄膜感測元件各項特性參數以獲得較佳之感測度、線性度與電容值。

2. 材料與方法

本研究之基板材料採用具耐酸鹼、疏水性佳且成本低之鈦 (Titanium, Ti) 基板，此鈦基板經 RCA 清洗流程清洗後，於鹽酸溶液中進行基板表面粗糙化，接著進行基板封裝。於實驗中所使用之電解液，係由 10mM 氯化釕 (Ruthenium Chloride, $RuCl_3$) 及 0.1M 氯化鉀 (Potassium Chloride, KCl) 混合之水溶液進行調配，將調配完成之溶液靜置 24 小時後備用。

氧化釕薄膜感測元件利用循環伏安法備製氧化釕薄膜於鈦基板上，採用三極式

系統，如圖一所示，以銀 / 氯化銀電極 (Ag/AgCl Electrode) 作為參考電極 (Reference Electrode)，並以鉑 (Platinum, Pt) 為對應電極 (Counter Electrode)，鈦基板為工作電極。且於 10mM 氯化釕及 0.1M 氯化鉀混合之水溶液於環境溫度 50℃進行沉積，並加入磁石攪拌以避免電解液產生沉澱現象，使薄膜沉積更佳均勻。將備製完成之氧化釕薄膜，進行退火處理，退火溫度分別為 100℃、150℃與 200℃，並探討氧化釕薄膜感測元件之最佳退火溫度。



圖一 三極式分析系統之示意圖。

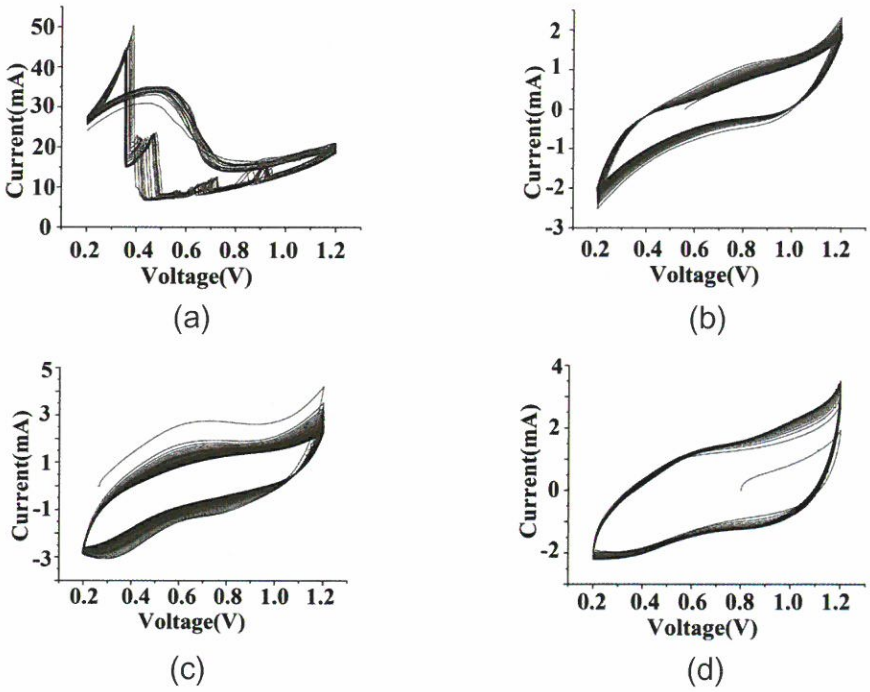
3. 結果與討論

(一) 探討以循環伏安法備製氧化釕薄膜感測元件之比電容值量測與分析

本研究以循環伏安法備製氧化釕薄膜感測元件，再以循環伏安法評估不同薄膜備製參數之擬電容行為及其比電容值變化。

本研究進行循環伏安量測實驗時，掃描電位介於 0.2V~1.2V、掃描速率為 50 mV/s、掃描圈數為 50 圈。圖二係分別未經退火處理、經 100℃、150℃與 200℃退火處理 10

分鐘後之循環伏安量測實驗結果圖，實驗結果顯示鈦片基材本身幾乎不具有電容特性，而其他經過退火處理之元件以循環伏安掃描 10 圈測試後，其循環伏安曲線於 0.2V~1.2V 之電位範圍內均呈現出陰陽極區域相當對稱之矩形，由實驗結果得知此方法備製之氧化釕薄膜感測元件，具有優異之擬電容特性以及氧化還原反應之可逆性。



圖二 以循環伏安法備製氧化釕薄膜感測元件 (a) 未退火處理、(b) 經 100℃ 退火處理、(c) 經 150℃ 退火處理與 (d) 經 200℃ 退火處理，其退火時間皆為 10 分鐘之循環伏安曲線圖。

另外亦藉由循環伏安量測結果以 Microsoft Origin 7.0 軟體計算各退火處理參數下備製之氧化釕薄膜感測元件之擬電容值與比電容值，其計算結果如表一所示，其中經 200℃ 退火處理之氧化釕薄膜感測元件量測循環伏安曲線所圍成面積較大，即代表擁有較高之能量儲存能力，擬電容值高達 600 mC，其比電容值高達 375 F/g。

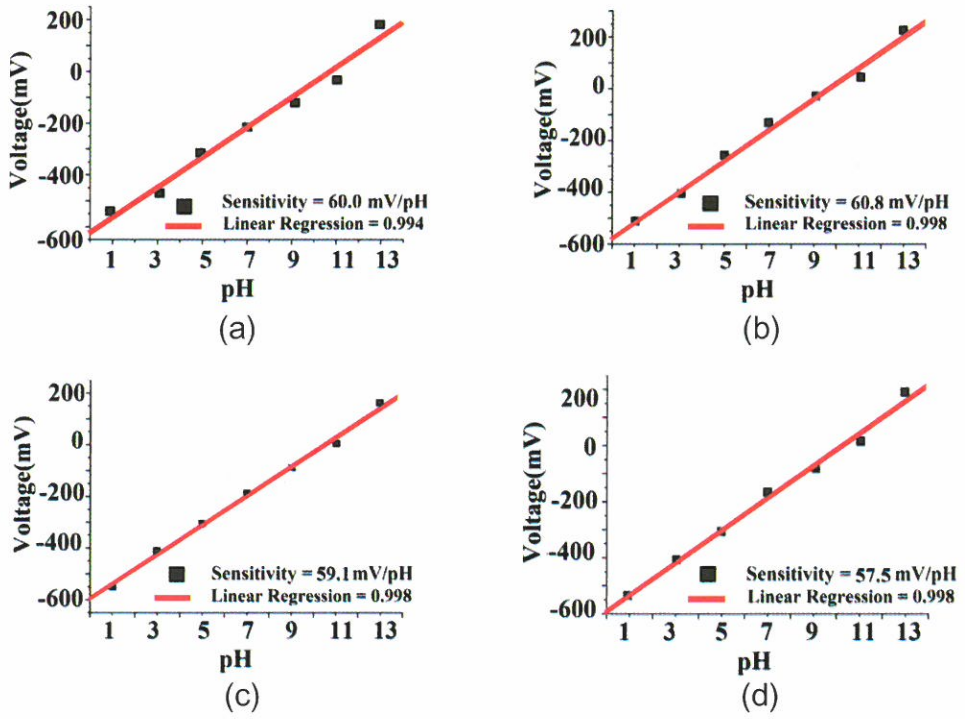
表一 氧化釕薄膜感測元件於不同退火溫度處理之電容值

元件之參數	比電容值F/g	擬電容值mC
未退火處理	-	5
經100℃退火處理	330	594
經150℃退火處理	344	413
經200℃退火處理	375	600

備註：符號「-」表示無法量測。

(二) 探討以循環伏安法備製氧化釕薄膜感測元件之感測特性分析

本研究係採用 V-T 量測系統將循環伏安法備製之氧化釕薄膜感測元件進行探討，分別為未退火處理、100℃、150℃與 200℃退火處理共 4 支元件，置放於不同酸鹼度之待測溶液中進行實驗，如圖三所示分別係上述 4 支氧化釕薄膜感測元件之感測特性曲線圖。



圖三 以循環伏安法備製氧化釕薄膜感測元件 (a) 未退火處理、(b) 經 100℃退火處理、(c) 經 150℃退火處理與 (d) 經 200℃退火處理，其退火時間皆為 10 分鐘之感測特性曲線圖。

所得之實驗數據再以 Microsoft Origin 7.0 軟體進行分析。由實驗結果得知以循環伏安法備製氧化釕薄膜感測元件中，未退火處理之氧化釕薄膜感測元件，其線性度較低，經退火處理之氧化釕薄膜感測元件，其感測度可達 57.5 mV/pH~ 60.8 mV/pH，且線性度可達 0.998，與相關文獻 [6, 7] 比較可得知本研究之氧化釕薄膜感測元件的感測度較為優異，表二係與相關文獻比較之彙整表。

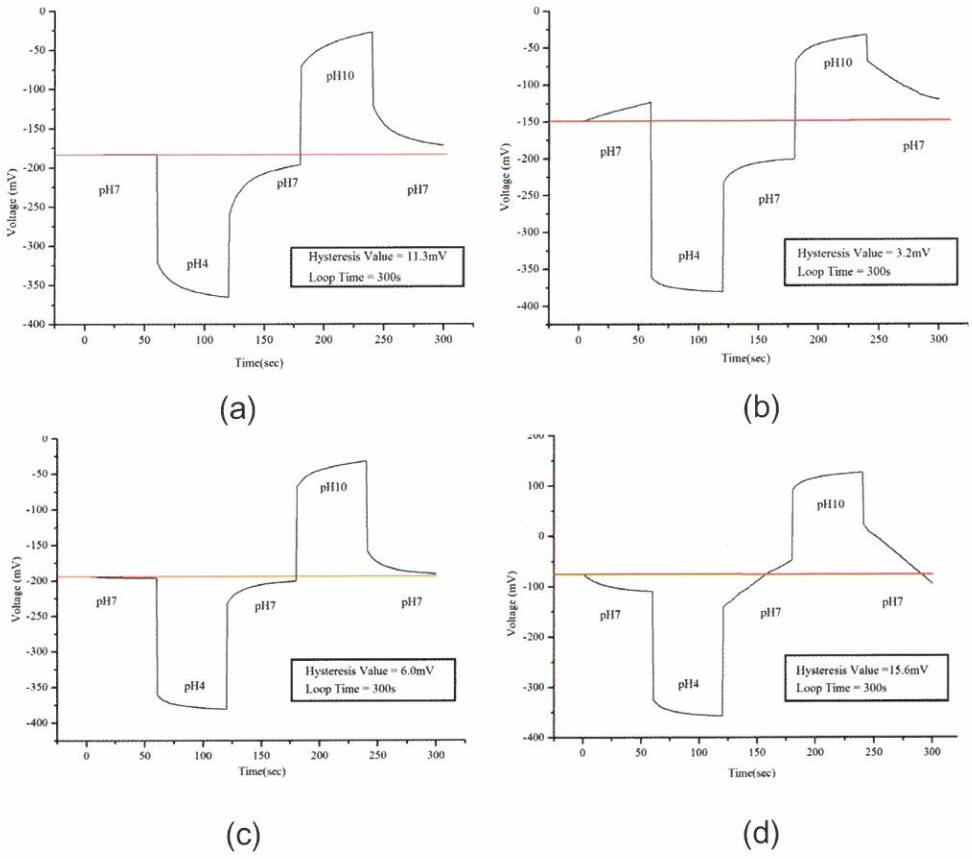
表二 本研究備製之氧化釕薄膜感測元件之特性參數與相關文獻比較

感測元件		感測度(mV/pH)	線性度
RuO_2	未退火處理	60.0	0.994
	100℃退火處理	60.8	0.998
	150℃退火處理	59.1	0.998
	200℃退火處理	57.5	0.998
RuO_2[6]		50.9	-
RuO_2[7]		51.2	-

備註：符號「-」表示未提供。

(三) 探討以循環伏安法備製氧化釕薄膜感測元件之非理想效應分析

本研究係採用 V-T 量測系統進行遲滯實驗，將所備製之氧化釕薄膜感測元件進行退火處理，分別為未退火處理、100℃、150℃與 200℃退火處理共 4 支元件，量測之待測溶液迴路為 pH7 → pH4 → pH7 → pH10 → pH7，迴路時間 (Loop Time) 為 300 秒，遲滯曲線圖依序呈現於圖四。



圖四 氧化釕薄膜感測元件於量測迴路 pH7 → pH4 → pH7 → pH10 → pH7 待測溶液之遲滯曲線圖 (a) 未退火處理、(b) 經 100℃ 退火處理、(c) 經 150℃ 退火處理與 (d) 經 200℃ 退火處理。

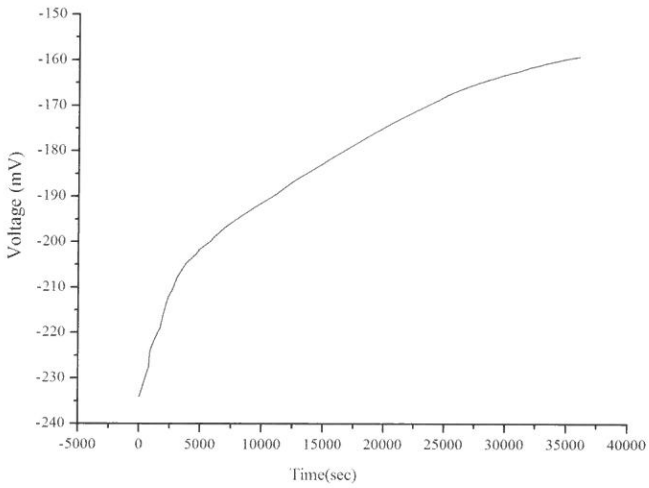
將遲滯實驗結果彙整如表三所示。從表三中可發現以 100℃ 退火處理之氧化釕薄膜感測元件有較小之遲滯量，但穩定度卻不佳。

綜合上述實驗結果得知以 150℃退火處理之感測元件擁有低遲滯效應之特性，並且具備良好之感測度與線性度，其中以 200℃退火處理之感測元件，雖亦擁有良好感測度與線性度，並且具備高電容性，但其遲滯效應過高，導致元件穩定性下降，故較不適用於離子感測，因此本研究之實驗結果呈現最佳製程參數，係以循環伏安法備製氧化釕薄膜經 150℃退火處理之感測元件，故本研究最後以最佳製程參數備製之感測元件，進行時漂實驗之探討。

表三 以循環伏安法備製氧化釕薄膜感測元件於不同退火溫度處理之遲滯量

退火溫度	迴路路徑	遲滯量
未退火	pH7 → pH4→ pH7 → pH10 → pH7	11.3mV
100℃退火處理	pH7 → pH4→ pH7 → pH10 → pH7	3.2mV
150℃退火處理	pH7 → pH4→ pH7 → pH10 → pH7	6.0mV
200℃退火處理	pH7 → pH4→ pH7 → pH10 → pH7	15.6mV

本研究最後採用 V-T 量測系統進行時漂量測實驗，將經 150℃退火處理之氧化釕薄膜感測元件進行實驗，於待測液 pH7 中量測，量測實驗係 10 小時，於實驗第 5 小時之數值為 -177.9 mV，實驗第 10 小時之數值為 -159.2mV，將實驗結果利用 Microsoft Origin 7.0 軟體繪製圖形，如圖五所示，其時漂率為 3.7 mV/hour。



圖五 氧化釕薄膜感測元件之時漂效應圖形。

由圖五得知以循環伏安法備製氧化釕薄膜感測元件經 150℃ 退火處理之氧化釕薄膜感測元件，其時漂率為 3.7 mV/hour，且與文獻 [10, 11] 比較可得知本研究之氧化釕薄膜感測元件的感測度、時漂率較為優異且感測元件亦較為穩定，表四係與文獻比較之彙整表。

表四 本研究備製之氧化釕薄膜感測元件之感測度及時漂率與相關文獻比較

感測元件	感測度(mV/pH)	時漂率(mV/hour)	基板
RuO_2[本研究]	59.1	3.7	鈦基板
SnO_2[10]	57.36	6.7	矽基板
SnO_2/ITO [11]	57	9.1	玻璃基板

4. 結論

本研究係以鈦基板作為氧化釕薄膜感測元件之基板，經過 150℃退火處理之氧化釕薄膜感測元件其最佳感測度為 59.1mV/pH、線性度為 0.998，與相關文獻比較後可得知本研究之氧化釕薄膜感測元件於酸鹼量測上具有良好之感測度、線性度及量測範圍廣泛之優勢。以循環伏安法備製之氧化釕薄膜感測元件於 200℃退火處理有最佳電容值，其比電容值為 375 F/g，擬電容值為 600 mC，故未來可改良其元件架構，發展成為薄膜式電容器。

本研究使用循環伏安法備製氧化釕薄膜感測元件，其具備備製過程簡單、設備操作簡易與備製參數易控制等優點，故往後可延伸應用至其他離子與酵素之量測，並且朝向微小化感測元件發展。

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Fabrication of High Capacitance Porous RuO_2 Hydrogen Ion Sensor

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Abstract

In this study, the porous high capacitance of RuO_2 thin film was fabricated as the working electrode of sensors by using cyclic voltammetry of electrochemistry deposition. These methods have the advantages of fabricated quickly and low cost. RuO_2 thin film has high conductance, high surface area and good electrochemistry reversibility. In addition, it possesses high stability and electrocatalysis characteristic in the acidic solution. Therefore, the surface structure of ruthenium oxide thin film was able to promote the porous and surface area of electrode and to increase the contact area between the ruthenium oxide film and buffer solution. The working electrode of RuO_2 thin film was achieved to high linearity, sensitivity and stability. Furthermore, this working electrode can apply to sense the hydrogen ions.

Key words: Porous, High Capacitance, Cyclic Voltammetry, Ruthenium Oxide, Hydrogen Ions

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A Comparative Study of Estimators for the Process Capability Index C''_{pk}

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Abstract

For processes with asymmetric tolerances, Pearn and Chen (1998) proposed a generalization index C''_{pk}. Some properties of the natural estimator of C''_{pk} under normality were discussed in Pearn at al. (2004). In this paper, we propose some indirect estimators of C''_{pk} based on the results in Singh and Saxena (2005). Asymptotic properties of the estimators are discussed. In addition, comparison among six estimators are made. A numerical study based on some combinations of parameters was conducted for the comparison between the proposed indirect estimators and the maximum likelihood estimator which was proposed by Pearn and Chen. It is found that for capable to very capable processes, indirect estimators which we proposed perform better than the natural MLE most of the time. The results of the current research can also be applied to improve acceptance sampling plan when a modied MIL-STD-1916 is considered.

Key words: Indirect estimator; Asymptotic unbiased; Consistent estimator.

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1. Introduction

In real world, it is not uncommon that there are some given enginnering specifications on the process characteristics. In a stable production process, to monitor whether a manufacturing process meets a preset level of production tolerance, the idea of detecting a process via a unitless numerical measure was proposed. A common summary quantitative measure is the process capability index. It has been used extensively in many different fields for the purpose of process assessment and improvement for suppliers and customers. Many process capability indices have been proposed in the literature since Juran *et al.* (1974) first proposed the idea. See Kotz and Johnson (1993), Bothe (1997), Kotz and Lovelace (1998) and references from there in.

The first well recognized process capability index C_p was proposed by Juran *et al.* (1974), where

$$C_p = \frac{\text{allowable range of measurements}}{\text{actual range of measurements}} = \frac{USL - LSL}{6\sigma}$$

and USL and LSL are the upper and the lower specification limit, respectively, σ is the process standard deviation.

Kane (1986) proposed an estimator $\widehat{C_p} = \frac{USL-LSL}{6S}$ for C_p by replacing the unknown parameter μ and σ by their consistent estimators $\bar{X}$ and S, respectively, where $\bar{X} = \frac{\sum_{i=1}^{n} X_i}{n}$ and $S = \sqrt{\frac{\sum_{i=1}^{n}(X_i-\bar{X})^2}{n-1}}$. However, as pointed out in Singh and Saxena (2005), based on the experiences from handling parameters in the past, one may have some prior information in the form of either a point, an interval or in the form of prior distribution. A class of shrinkage estimators $\widehat{C_p^S}$ was therefore propsoed for C_p when apriori or guessed value of standard deviation σ is available. Subsequently, the Bayesian estimators $\widehat{C_p^{B1}}$ and $\widehat{C_p^{B2}}$ of C_p had been done under squared error loss function by assuming particular quasi-prior distributions of (μ, σ) (Box and Tiao (1973)), and $(\mu, 1/\sigma)$ (Jeffreys (1961)). Except the estimators mentioned above, an unbiased estimator $\widehat{C_p^U}$ and a minimum mean squared error estimator $\widehat{C_p^M}$ for C_p in a class of linear estimators of the form proportional to the inverse of sample standard deviation were also provided.

In reality, however, most companies do not rely only on C_p to quantify process capability because it measures potential capability by the actual process spread only and does not take process shift into account. To solve the problem, Kane (1986) proposed the index C_{pk} that

$$C_{pk} = \frac{d_* - |\mu - M|}{3\sigma},$$

where μ and σ are the process mean and process standard deviation, respectively, $d_* = (USL - LSL)/2$ is the half length and $M = (USL + LSL)/2$ is the midpoint of the specification interval (LSL, USL).

Although C_{pk} is so widely used in practice, it makes no clear distinction between on-target ($\mu = T$) and off-target processes ($\mu \neq T$). On the other hand, even a process is on target, the tolerance may not be symmetric (i.e. the target value T is not at the midpoint M of the specification interval (LSL, USL)). Several generalizations of C_{pk} were proposed to handle the problem about asymmetric tolerances, e.g. C^*_{pk}, C'_{pk} and S_{pk}. However, these generalizations either understate or overstate the process capability in many cases. Pearn and Chen (1998) modified the index and proposed a generalization which was denoted by C''_{pk}. The mean and variance of the natural estimator of C''_{pk} were derived under normality and it was shown that C''_{pk} is superior to the existing generalizations of C_{pk}. In 2004, Pearn *et al.* investigated the relation between the fraction non-conforming and the value of C''_{pk} under normality. The explicit forms of the cumulative distribution function and the probability denstiy function for the natural esitmator were derived. Furthermore, they developed a decision making rule based on the natural estimator $\hat{C}''_{pk}$, which can be used to test whether a process is capable or not. Chen and Tsai (2012) derived the density function of the natural estimator from another approach. The expression of the density is in terms of finite sum and only involves standard normal distribution, and is easier to handle than the one given in Pearn et al. (2004).

Throughout the presentation of this paper, all developements are made assuming the process is in a state of statistical control and the characteristic under investigation arises from a normal distribution with mean μ and standard deviation σ. By re-expressing the form of the index C''_{pk}, several indirect estimators of the index are proposed. Asymptotic properties of these estimators are discussed.

The rest of this paper is organized as follows: In section 2, the index C''_{pk} is

reviewed, and six indirect estimators of C''_{pk} are proposed. Some inferential properties are derived. In section 3, comparisons among indirect estimators and MLE are made. In section 4, extensive calculation is performed to obtain better idea about optimal estimator with varies levels of C''_{pk}. Concluding remarks are given in section 5.

2. Process capability index C''_{pk}

The process capability index C_{pk} is widely used in real world, however, even if a process is on target, there are occasions that deviation of a quality characteristic from the ideal target in one direction is more tolerable than in the opposite direction. For example, the time to complete a special service in service industries, the size of baggages which are checked in by flight attendants, or the air which is pumped into the bag in food packaging are all designed to have unbalanced tolerance. To remedy this deficiency, Pearn and Chen (1998) proposed a generalization C''_{pk} of C_{pk} and is defined formally by

$$C''_{pk} = \frac{d^* - A^*}{3\sigma},$$

where

$$d^* = min\{D_u, D_l\}, \quad A^* = max\left\{\frac{d^*(\mu - T)}{D_u}, \frac{d^*(T - \mu)}{D_l}\right\},$$
$$and \quad D_u = USL - T, \; D_l = T - LSL.$$

Obviously, if T=M (symmetric tolerance), then $A^* = |\mu - T|$ and C''_{pk} is exactly the traditional index C_{pk}.

Notice that $C''_{pk} = \frac{d^* - A^*}{3\sigma}$ can be rewritten as

$$C''_{pk} = \frac{d^*}{3\sigma}\left[1 - \frac{A^*}{d^*}\right] \triangleq C''_p \dot{C}''_a,$$

where $C''_p = \frac{d^*}{3\sigma}$ measures the magnitude of the process variation, and $C''_a = \left[1 - \frac{A^*}{d^*}\right]$ measures the degree of process targeting. Note that $C''_a < 0$ only when the process mean μ is outside the specification interval (LSL, USL), and that won't happen when a process is under statistical control. In this study we therefore concern the cases when $C''_a = 1 - \frac{A^*}{d^*} \in [0, 1]$.

2.1 Indirect Estimators of C''_{pk}

Let $\widehat{\widehat{C''_p}}$ and $\widehat{\widehat{C''_a}}$ denote estimators of C''_p and C''_a, respectively. Then we call the estimator $\widehat{\widehat{C''_{pk}}} \triangleq \widehat{\widehat{C''_p}} \cdot \widehat{\widehat{C''_a}}$ an indirect estimator of the process capability index C''_{pk}. When $\widehat{\widehat{C''_p}} = \dfrac{d^*}{3S} \triangleq \widehat{C''_p}$ and $\widehat{\widehat{C''_a}} = 1 - \dfrac{\hat{A}^*}{d^*} \triangleq \widehat{C''_a}$ with $\hat{\mu}$=sample mean, the first indirect estimator

$$\widehat{C''_{pk1}} = \frac{d^*}{3S}\left(1 - \frac{\widehat{A^*}}{d^*}\right) = \widehat{C''_p}\widehat{C''_a}$$

coincides with the natural estimator proposed by Pearn and Chen (1998).

In the real world, not necessarily that all process measures follow normal distribution, however, the normal distribution is well known, has nice statistical properties, and can often be fitted to transfromed data even if it is not fit the original measurement all that well. For this main reason, the normal distribution will be assumed in this study.

Theorem 1 Let $X_1, \cdots, X_n$ be a random sample from $N(\mu, \sigma^2)$. Then
(a) $\widehat{C''_{pk1}}$ *is unbiased if and only if*

$$max\left\{\frac{\mu - T}{D_u}, \frac{T - \mu}{D_l}\right\} = 1 - \sqrt{\frac{n-1}{2}} \cdot \frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \cdot \left\{1 - \frac{\sigma}{\sqrt{n}} \cdot \left[(a+b)\cdot[\delta\Phi(\delta) + \phi(\delta)] - b\delta\right]\right\}.$$

where $\Gamma(x) = \int_0^\infty t^{x-1}e^{-t}dt, \quad x \in (0, \infty), a = \frac{1}{D_u}, b = \frac{1}{D_l}$ *and* $\delta = \frac{\mu - T}{\sigma/\sqrt{n}}$.
(b) $\widehat{C''_{pk1}}$ *is asymptotically unbiased.*
(c) $\widehat{C''_{pk1}}$ *is a consistent estimator of* C''_{pk}.

proof:

By Lemma 1, 2 given in the Appendix the Stirling's formula,

$$E(\widehat{C''_{pk1}}) = C''_p\, b_f^{-1}\left[1 - \frac{\sigma}{\sqrt{n}}\{(a+b)[\delta\Phi(\delta)+\phi(\delta)] - b\delta\}\right],$$

implies that the bias of $\widehat{C''_{pk1}} = \left\{\sqrt{\frac{n-1}{2}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\cdot\frac{E(\widehat{C''_a})}{C''_a} - 1\right\}\cdot C''_{pk} \overset{n\to\infty}{\longrightarrow} 0.$

$$Var(\widehat{C''_{pk1}}) = C''^2_p\left\{\left[(a+b)\left\{\left(\frac{n-1}{n-3}\right)\frac{\sigma^2}{n}(a-b)(\delta^2+1) - \frac{2\sigma\delta}{\sqrt{n}}\left(\frac{n-1}{n-3} - \frac{1}{b_f^2}\right)\right.\right.\right.$$
$$\left.\left.\left. + \frac{2b\delta^2\sigma^2}{n\, b_f^2}\right\}\right]\Phi(\delta) + \left[(a+b)\left\{\left(\frac{n-1}{n-3}\right)\frac{\sigma^2}{n}(a-b)\delta - \frac{2\sigma}{\sqrt{n}}\left(\frac{n-1}{n-3} - \frac{1}{b_f^2}\right) + \frac{2b\delta\sigma^2}{n\, b_f^2}\right\}\right]\phi(\delta)$$
$$- \frac{\sigma^2}{n\, b_f^2}(a+b)^2[\delta\Phi(\delta)+\phi(\delta)]^2 + \left(\frac{n-1}{n-3}\right)\frac{b^2\sigma^2}{n} + \left(\frac{n-1}{n-3} - \frac{1}{b_f^2}\right)\left(1 + \frac{b\delta\sigma}{\sqrt{n}}\right)^2\Bigg\}$$
$$\overset{n\to\infty}{\longrightarrow} 0. \ \square$$

In 2005, Singh and Saxena re-expressed the index as $C_p \triangleq K\theta$ where $\theta = 1/\sigma$, and proposed estimators of C_p other than the one given by Kane, namely the unbiased estimator $\widehat{C_p^U}$, the minimum mean square error estimator $\widehat{C_p^M}$ in a class of linear estimators, a class of shrinkage estimator $\widehat{C_p^S}$ that based on a class of estimators $\hat{\theta}_{(u,v)}$ of θ which minimizes the mean squared error (MSE). Sometimes the guessed value θ_0 may depart from the true θ, but by choosing appropriate parameters u and v, the shrinkage estimator $\widehat{C_p^S}$ can still perform well; The Bayes estimator $\widehat{C_p^{B1}}$ based on the class of quasi prior proportionate to $(1/\sigma)^c$ given in Box and Tiao (1973), and the Bayes estimator $\widehat{C_p^{B2}}$ based on the Jeffrey's (1961) quasi prior that proportionate to $(\sigma)^d$, for $c, d > 0$. When c=0 and d=2, the estimators $\widehat{C_p^{B1}}$ and $\widehat{C_p^{B2}}$ coincide with the unbiased estimator $\widehat{C_p^U}$. Likewise, the minimum mean square error estimator $\widehat{C_p^M}$ is the same as $\widehat{C_p^{B2}}$ when d=3, and the two Bayes estimators of C_p are the same when c=d=1. Comparisons among these estimators were also given in Singh and Saxena (2005) which indicate that for small sample size, the shrinkage estimator $\widehat{C_p^S}$ has the least mean square error. See Table 1.

Substitute $\widehat{\widehat{C''_p}}$ by the estimators given in Singh and Saxena (2005), five additional estimators of the process capability index C''_{pk} are given as the following:

$$\widehat{C''_{pk2}} = \left(\frac{d^*}{d_*}\right)\widehat{C_p^U}\cdot\widehat{C''_a} = \frac{d^*}{3S}\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1}{2})}{\Gamma(\frac{n-2}{2})}\cdot\widehat{C''_a} = \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1}{2})}{\Gamma(\frac{n-2}{2})}\cdot\widehat{C''_{pk1}},$$

$$\widehat{C''_{pk3}} = \left(\frac{d^*}{d_*}\right)\widehat{C_p^M}\cdot\widehat{C''_a} = \frac{d^*}{3S}\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-3}{2})}\cdot\widehat{C''_a} = \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-3}{2})}\cdot\widehat{C''_{pk1}},$$

$$\widehat{C''_{pk4}} = \left(\frac{d^*}{d_*}\right)\widehat{C_p^S}\cdot\widehat{C''_a} = \frac{d^*}{3S}[v\theta_0\cdot S\cdot(1-W'_{(n,u)}) + \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1}{2})}{\Gamma(\frac{n-2}{2})}\cdot W'_{(n,u)}]\cdot\widehat{C''_a}$$

$$= [v\theta_0\cdot S\cdot(1-W'_{(n,u)}) + \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1}{2})}{\Gamma(\frac{n-2}{2})}\cdot W'_{(n,u)}]\cdot\widehat{C''_{pk1}},$$

where $W'_{(n,u)} = \left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^u \frac{\Gamma(\frac{n-u-1}{2})}{\Gamma(\frac{n-2u-1}{2})}$, and $u \neq 0, v > 0$.

$$\widehat{C''_{pk5}} = \left(\frac{d^*}{d_*}\right)\widehat{C_p^{B1}}\cdot\widehat{C''_a} = \frac{d^*}{3S}\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+c-1}{2})}{\Gamma(\frac{n+c-2}{2})}\cdot\widehat{C''_a} = \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+c-1}{2})}{\Gamma(\frac{n+c-2}{2})}\cdot\widehat{C''_{pk1}}, \quad c \geq 0.$$

$$\widehat{C''_{pk6}} = \left(\frac{d^*}{d_*}\right)\widehat{C_p^{B2}}\cdot\widehat{C''_a} = \frac{d^*}{3S}\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-d+1}{2})}{\Gamma(\frac{n-d}{2})}\cdot\widehat{C''_a} = \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-d+1}{2})}{\Gamma(\frac{n-d}{2})}\cdot\widehat{C''_{pk1}}, \quad d > 0.$$

Motivated by the estimators given above, it can be seen that four of them are contained in a class of estimator in the form of

$$\widehat{C''_{pkl}} = \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})}\cdot\widehat{C''_{pk1}}.$$

i.e. In the case when $l \in \{2, 3, 2-c, d\}$, where $c \in \{1, 2, \ldots, 5\}$ and $d \in \{0, 1, 4, 5\}$, the estimator $\widehat{C''_{pkl}}$ becomes $\widehat{C''_{pk2}}$, $\widehat{C''_{pk3}}$, $\widehat{C''_{pk5}}$, $\widehat{C''_{pk6}}$, respectively.

Properties of these estimators are given in the following theorems. Part (a)(c)(d) of each theorem are based on Lemma 1, Lemma 2 and Stirling's formula. Part (e) can be proved by Markov inequality.

Theorem 2 Let $X_1, \cdots, X_n$ be a random sample from $N(\mu, \sigma^2)$. Then

(a) $E\left(\widehat{C''_{pkl}}\right) = C''_p\frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\left[1-\frac{\sigma}{\sqrt{n}}\{(a+b)[\delta\Phi(\delta)+\phi(\delta)]-b\delta\}\right]$.

(b) $\widehat{C''_{pkl}}$ is unbiased *if and only if*

$$max\left\{\frac{\mu-T}{D_u}, \frac{T-\mu}{D_l}\right\} = \frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})}\cdot\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\cdot\left\{1-\frac{\sigma}{\sqrt{n}}\cdot\left[(a+b)\cdot[\delta\Phi(\delta)+\phi(\delta)]-b\delta\right]\right\}.$$

(c) $\widehat{C''_{pkl}}$ is asymptotically unbiased.

(d) $Var(\widehat{C''_{pkl}})$

$$= C''^2_p \left(\frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})}\right)^2 \left\{ \left(\frac{2}{n-3} - \left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^2\right)\left(1+\frac{b\delta\sigma}{\sqrt{n}}\right)^2 + \left(\frac{2}{n-3}\right)\frac{b^2\sigma^2}{n}\right.$$

$$+(a+b)\left[\left(\frac{2}{n-3}\right)\frac{\sigma^2}{n}(a-b)(\delta^2+1) - \frac{2\delta\sigma}{\sqrt{n}}\left(\frac{2}{n-3} - \left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^2\right) + \frac{2b\delta^2\sigma^2}{n}\left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^2\right]\Phi(\delta)$$

$$+(a+b)\left[\left(\frac{2}{n-3}\right)\frac{\sigma^2}{n}(a-b)\delta - \frac{2\sigma}{\sqrt{n}}\left(\frac{2}{n-3} - \left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^2\right) + \frac{2b\delta\sigma^2}{n}\left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^2\right]\phi(\delta)$$

$$\left. - \frac{\sigma^2}{n}\left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^2 (a+b)^2[\delta\Phi(\delta)+\phi(\delta)]^2\right\} \quad \stackrel{n\to\infty}{\longrightarrow} 0.$$

(e) $\widehat{C''_{pkl}}$ is a consistent estimator of C''_{pk}.

proof:

(b) $bias(\widehat{C''_{pkl}}) = \left(\frac{\Gamma(\frac{n-d+1}{2})}{\Gamma(\frac{n-d}{2})} \cdot \frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \cdot \frac{E(\widehat{C''_a})}{C''_a} - 1\right) \cdot C''_{pk}$. □

Theorem 3 Let $X_1, \cdots, X_n$ be a random sample from $N(\mu, \sigma^2)$. Then

(a) $E\left(\widehat{C''_{pk4}}\right) = \left[\frac{d^*}{3}v\theta_0(1-W'_{(n,u)}) + W'_{(n,u)}C''_p\right] \cdot \left[1 - \frac{\sigma}{\sqrt{n}}\{(a+b)[\delta\Phi(\delta)+\phi(\delta)] - b\delta\}\right]$

(b) $\widehat{C''_{pk4}}$ is unbiased *if and only if*

$$max\left\{\frac{\mu - T}{D_u}, \frac{T-\mu}{D_l}\right\} = \left\{\frac{d^*}{3C''_p}v\theta_0\left[1 - \left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^u \frac{\Gamma(\frac{n-u-1}{2})}{\Gamma(\frac{n-2u-1}{2})}\right] + \left[\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right]^u \frac{\Gamma(\frac{n-u-1}{2})}{\Gamma(\frac{n-2u-1}{2})}\right\}$$

(c) $\widehat{C''_{pk4}}$ is asymptotically unbiased.

(d) $Var(\widehat{C''_{pk4}})$

$$= C''^2_p W'^2_{(n,u)}\left\{(a+b)\left[\left(\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})}\right)\frac{\sigma^2}{n}(a-b)(\delta^2+1) - \frac{2\delta\sigma}{\sqrt{n}}\left(\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})} - 1\right)\right.$$

$$\left. + \frac{2b\delta^2\sigma^2}{n}\right]\Phi(\delta) + (a+b)\left[\left(\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})}\right)\frac{\sigma^2}{n}(a-b)\delta - \frac{2\sigma}{\sqrt{n}}\left(\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})} - 1\right)\right.$$

$$\left. + \frac{2b\delta\sigma^2}{n}\right]\phi(\delta) - \frac{\sigma^2}{n}(a+b)^2[\delta\Phi(\delta)+\phi(\delta)]^2 + \left(\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})}\right)\frac{b^2\sigma^2}{n}$$

$$+\left(\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})} - 1\right)\left(1+\frac{b\delta\sigma}{\sqrt{n}}\right)^2\Big\} + \left[\frac{1}{9}d^{*2}v^2\theta_0^2(1-W'_{(n,u)})^2 + \frac{2}{3}d^*v\theta_0(1-W'_{(n,u)})C''_p\right] \cdot$$

$$\left[\frac{\sigma^2}{n}\left\{[(a+b)^2\delta^2 + (a^2-b^2)]\Phi(\delta) + (a+b)^2\delta\phi(\delta) + b - (a+b)^2[\delta\Phi(\delta)+\phi(\delta)]^2\right\}\right] \quad \stackrel{n\to\infty}{\longrightarrow} 0,$$

(e) $\widehat{C''_{pk4}}$ is a consistent estimator of C''_{pk}.

proof:

(b) $bias(\widehat{C''_{pk4}})$

$= \left(\left\{ \frac{d^*}{3C''_p} v\theta_0 \left[1 - \left[\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \right]^u \frac{\Gamma(\frac{n-u-1}{2})}{\Gamma(\frac{n-2u-1}{2})} \right] + \left[\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \right]^u \frac{\Gamma(\frac{n-u-1}{2})}{\Gamma(\frac{n-2u-1}{2})} \right\} \cdot \frac{E(\widehat{C''_a})}{C''_a} - 1 \right) \cdot C''_{pk}$. □

3. Comparison Among Estimators of C''_{pk}

In this section, we report on a comparative study for the proposed indirect estimators based on the results from section 2. To make the comparisons, differences among the mean squared errors of estiamtors are needed. However, all the expressions of pairwise differences are very complicated. For example, the difference between the MSE of $\widehat{C''_{pk1}}$ and the MSE of $\widehat{C''_{pk2}}$, which is the simplest one within fifteen possible differences, is given by :

$$\begin{aligned}
&\text{MSE}(\widehat{C''_{pk1}}) - \text{MSE}(\widehat{C''_{pk2}}) \\
&= (C''_{pk})^2 \cdot \left\{ \frac{EC''_a}{C''_a} \cdot \{\frac{1}{b_f} - 1\} \cdot \{\frac{EC''_a}{C''_a} \cdot (\frac{1}{b_f} + 1) - 2\} \right\} + \left[\frac{n-1}{n-3} - \frac{n-3}{2} \cdot \left(\frac{\Gamma(\frac{n-3}{2})}{\Gamma(\frac{n-2}{2})} \right)^2 \right] \\
&\cdot \left\{ \frac{(a+b)\sigma}{\sqrt{n}} \cdot \left[\left(\frac{(a-b)\sigma(\delta^2+1)}{\sqrt{n}} - 2\delta \right) \cdot \Phi(\delta) + \left(\frac{(a-b)\sigma\delta}{\sqrt{n}} - 2 \right) \cdot \phi(\delta) \right] \right. \\
&\left. + \left(1 + \frac{b\delta\sigma}{\sqrt{n}} \right)^2 + \frac{(b\sigma)^2}{n} \right\} + (1 - \frac{1}{b_f^2}) \cdot \left[\frac{(a+b)\sigma}{\sqrt{n}} \cdot \left(\delta\Phi(\delta) + \phi(\delta) \right) + 1 + \frac{b\delta\sigma}{\sqrt{n}} \right]^2 .
\end{aligned}$$

As we can see from the equation, it is extremely complicated to decide the sign of the difference. Therefore, a different approach for comparison is required.

3.1 Comparison Without $\widehat{C''_{pk4}}$

As mentioned in previous section, $\widehat{C''_{pk2}}$, $\widehat{C''_{pk3}}$, $\widehat{C''_{pk5}}$, $\widehat{C''_{pk6}}$ can be represented as

$$\widehat{C''_{pk}}(t) = t \cdot \frac{d^*}{3S} \cdot (1 - \frac{\widehat{A^*}}{d^*}) = t \cdot \widehat{C''_{pk1}},$$

where $t = \sqrt{\frac{2}{n-1}} \cdot \frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})}$ with $l = 2, 3, 2-c$ and d, respectively.

For the case when $c \in \{1, 2, \ldots, 5\}$ and $d \in \{0, 1, 4, 5\}$, let

$$\widehat{C''_{pk}}(\gamma) = \gamma \cdot \frac{d^*}{3S} \cdot (1 - \frac{\widehat{A^*}}{d^*}) = \gamma \cdot \widehat{C''_{pk1}}$$

where $n \geq 6$ and

$$\gamma \in S = \{1\} \cup \{\sqrt{\frac{2}{n-1}} \cdot \frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})} \mid l = -3, -2, -1, 0, 1, 2, 3, 4, 5\}.$$

It is clear that

$$Var(\widehat{C''_{pk}}(\gamma)) = \gamma^2 \cdot Var(\widehat{C''_{pk1}})$$

$$\left|Bias(\widehat{C''_{pk}}(\gamma))\right|^2 = \left(E(\widehat{C''_{pk1}})\right)^2 \cdot \gamma^2 - 2C''_{pk}E(\widehat{C''_{pk1}}) \cdot \gamma + (C''_{pk})^2$$

and

$$\begin{aligned} MSE(\widehat{C''_{pk}}(\gamma)) &= \gamma^2 \cdot Var(\widehat{C''_{pk1}}) + \left(\gamma \cdot E(\widehat{C''_{pk1}}) - C''_{pk})\right)^2 \\ &= \left(Var(\widehat{C''_{pk1}}) + (E(\widehat{C''_{pk1}}))^2\right) \cdot \gamma^2 - 2C''_{pk}E(\widehat{C''_{pk1}}) \cdot \gamma + (C''_{pk})^2. \end{aligned}$$

Obviously, $Var(\widehat{C''_{pk}}(\gamma))$ increases in γ. On the other hand, denote $\gamma_l = \sqrt{\frac{2}{n-1}} \cdot \frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})}$, by Lemma 3, Lemma 4 and Lemma 5 in the Appendix, for $n \geq 6$,

$$\gamma_{-3} > \gamma_{-2} > \gamma_{-1} > \gamma_0 > 1 > \gamma_1 > \cdots > \gamma_5.$$

Since γ_4 and γ_5 correspond to the estimator $\widehat{C''_{pk6}}$ with $d = 4, 5$, it implies that $\widehat{C''_{pk6}}$ has the smallest variance among $\widehat{C''_{pki}}$, for $i = 1, 2, 3, 5, 6$ when $d > 3$. Also, γ_{-3}, γ_{-2} and γ_{-1} correspond to the estimator $\widehat{C''_{pk5}}$ with $c = 5, 4$ and 3, implies that $\widehat{C''_{pk5}}$ has the largest variance among $\widehat{C''_{nki}}$, for $i = 1, 2, 3, 5, 6$ when $c \geq 3$ That is

$$Var(\widehat{C''_{pk5}}|c=5,4,3) > Var(\widehat{C''_{pk5}}|c=2) = Var(\widehat{C''_{pk6}}|d=0)$$

$$> Var(\widehat{C''_{pk1}}) > Var(\widehat{C''_{pk5}}|c=1) = Var(\widehat{C''_{pk6}}|d=1)$$

$$> Var(\widehat{C''_{pk2}}) > Var(\widehat{C''_{pk3}}) > Var(\widehat{C''_{pk6}}|d=4,5).$$

For any real number x,

$$\left(E(\widehat{C''_{pk1}})\right)^2 x^2 - 2C''_{pk}E(\widehat{C''_{pk1}})x + (C''_{pk})^2$$

attains its minimum value 0 when $x = \frac{C''_{pk}}{E(\widehat{C''_{pk1}})}$. And

$$\left(Var(\widehat{C''_{pk1}}) + (E(\widehat{C''_{pk1}}))^2\right) x^2 - 2C''_{pk}E(\widehat{C''_{pk1}})x + (C''_{pk})^2$$

reaches its minimum value

$$\frac{Var(\widehat{C''_{pk1}})(C''_{pk})^2}{Var(\widehat{C''_{pk1}}) + (E(\widehat{C''_{pk1}}))^2}$$

when

$$x = \frac{C''_{pk}E(\widehat{C''_{pk1}})}{Var(\widehat{C''_{pk1}}) + (E(\widehat{C''_{pk1}}))^2}.$$

Therefore, $\left|Bias(\widehat{C''_{pk}}(\gamma))\right|^2$ approaches 0 when γ is very close to

$$\frac{C''_{pk}}{E(\widehat{C''_{pk1}})},$$

and $MSE(\widehat{C''_{pk}}(\gamma))$ approaches $\frac{Var(\widehat{C''_{pk1}})(C''_{pk})^2}{Var(\widehat{C''_{pk1}})+(E(\widehat{C''_{pk1}}))^2}$ when γ is very close to

$$\frac{C''_{pk}E(\widehat{C''_{pk1}})}{Var(\widehat{C''_{pk1}}) + (E(\widehat{C''_{pk1}}))^2}.$$

3.2 Comparison with $\widehat{C''_{pk4}}$

Let $\Delta = \frac{\theta_0}{\theta}$, then

$$\begin{aligned} MSE(\widehat{C''_{pk4}}) &= (W'_{(n,u)})^2 b_f^2 Var(\widehat{C''_{pk1}}) + r_1 \cdot r_2 \\ &+ \left\{ \left[v\Delta(1 - W'_{(n,u)}) + W'_{(n,u)} \right] b_f E(\widehat{C''_{pk1}}) - C''_{pk} \right\}^2 \end{aligned}$$

achieves its minimun at

$$(v\Delta)^* = \frac{b_f(E\widehat{C''_{pk1}})(C''_{pk}) - W'_{(n,u)} b_f^2 (E\widehat{C''_{pk1}})^2 - (C''_p)^2 r_2}{(1 - W'_{(n,u)}) \left[(C''_p)^2 r_2 + b_f^2 (E\widehat{C''_{pk1}})^2 \right]}, \tag{1}$$

where

$$r_1 = \left[(v\Delta)^2 (1 - W'_{(n,u)})^2 + 2(v\Delta)(1 - W'_{(n,u)}) \right] (C''_p)^2 > 0,$$

$$r_2 = b + (a^2 - b^2)\Phi(\delta) + (a+b)^2(\delta\Phi(\delta) + \phi(\delta))[\delta - (\delta\Phi(\delta) + \phi(\delta))],$$

$$a = \frac{1}{USL - T}, \quad b = \frac{1}{T - LSL}, \text{ and } \quad \delta = \sqrt{n}(\frac{\mu - T}{\sigma}).$$

When $W'_{(n,u)}$ is fixed, r_1 is determined by the values of v and Δ, r_2 is determined by the value of T and δ.

For $\gamma \in S$,

(1) $Var(\widehat{C''_{pk}}(\gamma)) < Var(\widehat{C''_{pk4}}) \Leftrightarrow \gamma < \sqrt{\frac{Var(\widehat{C''_{pk4}})}{Var(\widehat{C''_{pk1}})}}$.

For $r_2 < 0$, $Var(\widehat{C''_{pk4}}) < Var(\widehat{C''_{pk2}})$ when $u = -1$, and $Var(\widehat{C''_{pk4}}) < Var(\widehat{C''_{pk3}})$ when $u = 1$.

(2) $|Bias(\widehat{C''_{pk}}(\gamma))| < |Bias(\widehat{C''_{pk4}})|$

$\Leftrightarrow \frac{C''_{pk}}{E(\widehat{C''_{pk1}})} - \frac{|E(\widehat{C''_{pk4}}) - C''_{pk}|}{|E(\widehat{C''_{pk1}})|} < \gamma < \frac{C''_{pk}}{E(\widehat{C''_{pk1}})} + \frac{|E(\widehat{C''_{pk4}}) - C''_{pk}|}{|E(\widehat{C''_{pk1}})|}$.

(3) $MSE(\widehat{C''_{pk}}(\gamma)) < MSE(\widehat{C''_{pk4}})$

$$\Leftrightarrow \frac{C''_{pk}E(\widehat{C''_{pk1}})}{Var(\widehat{C''_{pk1}})+(E(\widehat{C''_{pk1}}))^2} - \sqrt{\frac{MSE(\widehat{C''_{pk4}})-\frac{Var(\widehat{C''_{pk1}})(C''_{pk})^2}{Var(\widehat{C''_{pk1}})+[E(\widehat{C''_{pk1}})]^2}}{Var(\widehat{C''_{pk1}})+[E(\widehat{C''_{pk1}})]^2}} < \gamma$$

$$< \frac{C''_{pk}E(\widehat{C''_{pk1}})}{Var(\widehat{C''_{pk1}})+(E(\widehat{C''_{pk1}}))^2} + \sqrt{\frac{MSE(\widehat{C''_{pk4}})-\frac{Var(\widehat{C''_{pk1}})(C''_{pk})^2}{Var(\widehat{C''_{pk1}})+[E(\widehat{C''_{pk1}})]^2}}{Var(\widehat{C''_{pk1}})+[E(\widehat{C''_{pk1}})]^2}}.$$

For the proposed estimators to be practical and convenience to use, a step-by-step procedure is provided as the following:

Step 1: Compare the standard error of $\widehat{C''_{pk4}}$ with the standard error of $\widehat{C''_{pk6}}$. (From 3.1, we already know that $\widehat{C''_{pk6}}$ with $d = 5$ has the smallest standard error.)

Step 2: (a) Among the five estimators $\widehat{C''_{pk1}}$, $\widehat{C''_{pk2}}$, $\widehat{C''_{pk3}}$, $\widehat{C''_{pk5}}$, $\widehat{C''_{pk6}}$, the estimator which corresponds to the γ that is closest to $\frac{C''_{pk}}{E(\widehat{C''_{pk1}})}$ has the smallest $|Bias|$.

(b) The estimator which corresponds to the γ that is closest to $\frac{C''_{pk}E(\widehat{C''_{pk1}})}{Var(\widehat{C''_{pk1}})+(E(\widehat{C''_{pk1}}))^2}$ has the smallest MSE.

Step 3: Compute the MSE and $|Bias|$ of the estimator $\widehat{C''_{pk4}}$.

Step 4: Compare the results from Step 2 and Step 3. The one with smallest MSE, or $|Bias|$ is the best estimator under corresponding comparison standard.

4. Numerical Study

In this section extensive calculation is performed to obtain better idea about op-

timal estimator under different situation with varies levels of C''_{pk}. Consider normal processes with asymmetric specification tolerances LSL=10, USL=50; To cover capable to very capable processes, let $C''_{pk} \in \{1, 1.33, 1.67, 2\}$; Performance of estimators for small to large sample are concerned, so choose sample size n from $\{6, 10, 30, 70, 100, 300, 500, 1000\}$. The process standard deviation $\sigma = 2.22, 2.49, 2.86, 3.33$ are selected.

The condition that $LSL < \mu < USL$ has been a minimum capability requirement applies to most start-up engineering applications or new processes. For the σ chosen, by Lemma 5 in the Appendix, to reach the required $C''_{pk} = 1.0$, (μ, T) must lie on the level curve as shown on Figure 1. Similarly, for $C''_{pk} = 1.33, 1.67.2.0$, (μ, T) must lie on the curve as shown on Figure 2, Figure 3, Figure 4, respectively. As we can see that the level curve is getting tighter when the capability index is getting larger for each fixed sigma. In this numerical study, some representative paris (μ, σ) are chosen for each specific index value.

For the shringkage estimator, take $u \in \{-1, 1\}$. Note that for different combinations of parameters, it is possible that $(v\Delta)^*$ becomes negative, which may lead to an undesirable negative $\widehat{C''_{pk4}}$. Therefore, the value "zero" will be assigned to $(v\Delta)^*$ when it happens. In the entire numerical study, there will be 32 different combinations for the case when $T = \mu$, and 468 different combinations for the case when $T \neq \mu$.

The computation result shows that for the comparison without $\widehat{C''_{pk4}}$, if the process is on target (i.e. $T = \mu$), then for all sample sizes, $\widehat{C''_{pk6}}$ with $d = 5$ has the smallest standard error; When the mean squared error MSE is compared, as the sample size n increases from 6 to 1000, the optimal estimators are $\widehat{C''_{pk3}}$, $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$, $\widehat{C''_{pk5}}$, respectively. And becomes $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$, $\widehat{C''_{pk5}}$, respectively, when the absolute bias $|BIAS|$ is used. See the 1st, 2nd, 5th and the 8th column in Table 2.

When the process is off target (i.e. $T \neq \mu$), again $\widehat{C''_{pk6}}$ with $d = 5$ has the smallest standard error; $\widehat{C''_{pk2}}$ has the smallest absolute bias; and $\widehat{C''_{pk3}}$ has the smallest mean squared error among the five indirect estimators. See the 1st, 2nd, 3rd, 4th, 9th and the 11th column in Table 3.

In the special case when $T = M$ (process with symmetric tolearnce), C''_{pk6} has the least standard error. The result depends on the distance D between μ and T if either MSE or $|BIAS|$ is used. When $D \leq 0.02$, for both on target and off target processes, if MSE is used, the optimal estimators for small to large sample are $\widehat{C''_{pk3}}$, $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$ $\widehat{C''_{pk5}}$, respectively. When $|BIAS|$ for each estimator is compared, the optimality when the sample size increases becomes $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$, $\widehat{C''_{pk5}}$. While $D > 0.02$, $\widehat{C''_{pk3}}$ has the smallest MSE; $\widehat{C''_{pk2}}$ has the smallest $|BIAS|$. See Table 4.

When the comparison includes $\widehat{C''_{pk4}}$, and if a process is on target, $\widehat{C''_{pk4}}$ has the smallest MSE; When $|BIAS|$ is considered, then the optimal estimators are $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$ $\widehat{C''_{pk5}}$, $\widehat{C''_{pk4}}$ when the sample size increases as above. $\widehat{C''_{pk6}}$ with $d = 5$ has the smallest standard error regardless the sample size; See the 1st, 3rd, 4th, 6th, 7th and the 8th column in Table 2.

When the process is off target, $\widehat{C''_{pk2}}$ has the least $|BIAS|$; and $\widehat{C''_{pk6}}$ has the smallest standard error; However, the situation changes when MSE is compared. When $C''_{pk} = 2$, $\widehat{C''_{pk4}}$ performs the best; For the other index value, there is no certain pattern, the optimality depends on the location of the target T and the sample size. See the 1st, 2nd, 5rd, 6th, 7th, 8th, 10th and the 11th column in Table 3.

For the case when $T = M$, $\widehat{C''_{pk6}}$ has the least standard error. For the other two standards, the results depend on the distance D between μ and T. When $D \leq 0.02$, for both $\mu \neq T$ and $\mu = T$, if MSE is considered, then as the sample size increases, the best estimators are $\widehat{C''_{pk4}}$, $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$, $\widehat{C''_{pk5}}$ for the case when $u = -1$; for $u = 1$, the best estimators are $\widehat{C''_{pk4}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$, $\widehat{C''_{pk5}}$; When use $|BIAS|$ as standard, the best estimators become $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$, $\widehat{C''_{pk1}}$, $\widehat{C''_{pk5}}$, $\widehat{C''_{pk4}}$. While $D > 0.02$, $\widehat{C''_{pk2}}$ has the smallest $|BIAS|$. For small sample size and large index, $\widehat{C''_{pk4}}$ has the least MSE. For all the other cases, $\widehat{C''_{pk3}}$ hs the smallest MSE almost all the way. See Table 4.

5. Conclusions

Pearn and Chen (1998) proposed a generalization C''_{pk} of C_{pk} to handle the situation when a process has asymmetric tolerance and a natural estimator was given. In this research, by assuming that a process follows a normal distribution, we propose more estimators of the process capability index C''_{pk}. The mean and variance of each estimator are derived, and it is shown that all these estimators are consistent and are all asymptotically unbiased. The absolute bias, standard error and mean squared errors of these estimators are derived.

However, even with all the analytical results about the absolute bias, standard error and mean squared errors for each estimator, it is still hopeless to derive the condition for the comparison. The comparison was discussed via an example. Under normality, the numerical computations shows that $\widehat{C''_{pk6}}$ has the smallest standard error under all circumstances. When we use $|Bias|$ as comaparison standard, and when the process is off target (i.e. $T \neq \mu$), $\widehat{C''_{pk2}}$ is the best estimator. However, when the process is on target (i.e. $T = \mu$), $\widehat{C''_{pk2}}$, $\widehat{C''_{pk6}}$ and $\widehat{C''_{pk1}}$ perform well for small sample. $\widehat{C''_{pk5}}$ performs the best for moderate to large sample, and $\widehat{C''_{pk4}}$ performs the best for extremely large sample. Finally, when we use the MSE as the comparison standard, $\widehat{C''_{pk4}}$ is the best when the process is on target (i.e. $T = \mu$). When the process is off target (i.e. $T \neq \mu$), $\widehat{C''_{pk3}}$ preforms better for smaller C''_{pk}, but $\widehat{C''_{pk4}}$ performs better for larger C''_{pk}. In conclusion, MLE is no longer the best among all possible estiamtors.

The last thing we would like to point out is about the standard MIL-STD-1916 which was published by US goverment. The purpose of such standard was to encourage those defence contractors and other commercial organizations who supplying goods and services to the U.S. Government to keep on improving the quality of their products. However, the MIL-STD-1916 is desinged based on the process capability index C_{pk}, which may not be proper for processes with asymmetric tolerance. Therefore, we suggest to modify the MIL-STD-1916 based on the estimators we proposed in this article to improve acceptance sampling plan. Such a modified standard should provide valuable information to those suppliers and US government when they have to face products with asymmetric tolerance.

Appendix

Lemma 1 Let $X_1, \cdots, X_n$ be a random sample from $N(\mu, \sigma^2)$. Then
(a) the pdf of $\widehat{C''_a}$ is defined by

$$f_{\widehat{C''_a}}(\widetilde{y}) = \frac{1}{\sigma\sqrt{2\pi}}\left(\frac{1}{a}e^{\frac{-1}{2}(\frac{1-\widetilde{y}}{a\sigma}-\delta)^2} + \frac{1}{b}e^{\frac{-1}{2}(\frac{1-\widetilde{y}}{b\sigma}+\delta)^2}\right),\ \widetilde{y} \le 1 \tag{1}$$

(a) By Lin(2005), $L^* = \widehat{A^*}/d^* = max\left\{\frac{\bar{X}-T}{D_u}, \frac{T-\bar{X}}{D_l}\right\}$ follows a generalized folded-normal distribution $N_F(\delta, n^{-1/2}\sigma; a, b)$, with the rth moment

$$E(L^{*r}) = \left(\frac{\sigma}{\sqrt{n}}\right)^r \cdot \sum_{j=0}^{r}\binom{r}{j}\delta^{r-j}\left[a^r\mathcal{I}_j(-\delta) + (-1)^{r-j}b^r\mathcal{I}_j(\delta)\right],$$

where

$$\mathcal{I}_j(\delta) = \int_{\delta}^{\infty}\mathbf{t}^j\phi(\mathbf{t})d\mathbf{t}.$$

This implies that the expected value of $\widehat{C''_a}$

$$E(\widehat{C''_a}) = E(1-L^*) = 1 - \frac{\sigma}{\sqrt{n}}\Big\{(a+b)[\delta\Phi(\delta)+\phi(\delta)] - b\delta\Big\}.$$

(b) $E(\widehat{C''_a}) = 1-\frac{\sigma}{\sqrt{n}}\Big\{(a+b)[\delta\Phi(\delta)+\phi(\delta)]-b\delta\Big\} \overset{n\to\infty}{\longrightarrow} C''_a = \begin{cases} \frac{USL-\mu}{USL-T} & \text{if } \mu > T \\ \frac{\mu-LSL}{T-LSL} & \text{if } \mu < T. \end{cases}$

□

Lemma 2 Let $X_1, \cdots, X_n$ be a random sample from $N(\mu, \sigma^2)$. Then
(a) the pdf of $\widehat{C''_p}$ is given by

$$f_{\widehat{C''_p}}(y) = \frac{(\frac{d^*}{d})^{n-1}(n-1)^{\frac{n-1}{2}}C_p^{n-1}}{\Gamma(\frac{n-1}{2})2^{\frac{n-3}{2}}}y^{-n}exp\left\{\frac{-(\frac{d^*}{d})^2(n-1)C_p^2}{2y^2}\right\}, y > 0 \tag{2}$$

with mean $E(\widehat{C''_p}) = \sqrt{\frac{n-1}{2}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \cdot C''_p$, where $C_p = d/3\sigma > 0$, and $n > 1$.
(b) $\widehat{C''_p}$ is an asymptotic unbiased estimator of C''_p.

proof:

(a) A natural estimator of C_p is defined by $\widehat{C_p} = d/3S$. By Chou and Owen (1989), for $n > 1$ the distribution of $\widehat{C_p}$ is

$$f_{\widehat{C_p}}(x) = \frac{(n-1)^{\frac{n-1}{2}} C_p^{n-1}}{\Gamma(\frac{n-1}{2})2^{\frac{n-3}{2}}} x^{-n} exp\left\{\frac{-(n-1)C_p^2}{2x^2}\right\}, \quad x > 0.$$

and $E(\widehat{C_p}) = \sqrt{\frac{n-1}{2}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \cdot C_p$.
Since $\widehat{C''_p} = \widehat{C_p} \cdot \frac{d^*}{d}$, it implies that the pdf of $\widehat{C''_p}$ is

$$f_{\widehat{C''_p}}(y) = \frac{(\frac{d^*}{d})^{n-1}(n-1)^{\frac{n-1}{2}} C_p^{n-1}}{\Gamma(\frac{n-1}{2})2^{\frac{n-3}{2}}} y^{-n} exp\left\{\frac{-(\frac{d^*}{d})^2(n-1)C_p^2}{2y^2}\right\}, y > 0.$$

and $E(\widehat{C''_p}) = \sqrt{\frac{n-1}{2}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})} \cdot C''_p$.

(b) By Stirling's formula. □

Lemma 3 For $l_2 > l_1$,

$$\frac{\Gamma(\frac{n-l_1+1}{2})}{\Gamma(\frac{n-l_1}{2})} > \frac{\Gamma(\frac{n-l_2+1}{2})}{\Gamma(\frac{n-l_2}{2})}.$$

Proof:

Note that for $x, y \in (0, \infty)$,

$$\int_0^1 v^{y-1}(1-v)^{x-1}dv = \frac{\Gamma(x)\Gamma(y)}{\Gamma(x+y)}.$$

Let $x = \frac{n-l}{2}, y = \frac{1}{2}$, then

$$\int_0^1 v^{\frac{1}{2}-1}(1-v)^{\frac{n-l}{2}-1}dv = \frac{\Gamma(\frac{n-l}{2})\Gamma(\frac{1}{2})}{\Gamma(\frac{n-l}{2}+\frac{1}{2})}.$$

Thus,

$$\frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})} = \frac{\Gamma(\frac{n-l}{2}+\frac{1}{2})}{\Gamma(\frac{n-l}{2})} = \Gamma(\frac{1}{2})\frac{1}{\int_0^1 v^{\frac{1}{2}-1}(1-v)^{\frac{n-l}{2}-1}dv}.$$

Since $(1-v)^{\frac{n-l}{2}-1}$ is an exponential function of $(\frac{n-l}{2}-1)$ and $0 < 1-v < 1$, for $l_2 > l_1$ one has

$$(1-v)^{\frac{n-l_2}{2}-1} > (1-v)^{\frac{n-l_1}{2}-1},$$

implies that

$$\int_0^1 v^{\frac{1}{2}-1}(1-v)^{\frac{n-l_2}{2}-1}dv > \int_0^1 v^{\frac{1}{2}-1}(1-v)^{\frac{n-l_1}{2}-1}dv,$$

and

$$\frac{1}{\int_0^1 v^{\frac{1}{2}-1}(1-v)^{\frac{n-l_2}{2}-1}dv} < \frac{1}{\int_0^1 v^{\frac{1}{2}-1}(1-v)^{\frac{n-l_1}{2}-1}dv}.$$

Hence,

$$\frac{\Gamma(\frac{n-l_1+1}{2})}{\Gamma(\frac{n-l_1}{2})} > \frac{\Gamma(\frac{n-l_2+1}{2})}{\Gamma(\frac{n-l_2}{2})}.$$

Lemma 4 (Wade 2004) If $x, y \in (0, \infty)$ then

$$\int_0^{\frac{\pi}{2}} \cos^{2x-1}\varphi \cdot \sin^{2y-1}\varphi d\varphi = \frac{\Gamma(x)\Gamma(y)}{2\Gamma(x+y)}.$$

Lemma 5

$$\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+1}{2})}{\Gamma(\frac{n}{2})} > 1 > \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n}{2})}{\Gamma(\frac{n-1}{2})}$$

Proof:

Let $x = \frac{n-l}{2}, y = \frac{1}{2}$, by Lemma 2,

$$\int_0^{\frac{\pi}{2}} \cos^{n-l-1}\varphi \cdot \sin^0\varphi d\varphi = \frac{\Gamma(\frac{n-l}{2})\Gamma(\frac{1}{2})}{2\Gamma(\frac{n-l}{2}+\frac{1}{2})} \Longrightarrow \frac{\Gamma(\frac{n-l+1}{2})}{\Gamma(\frac{n-l}{2})} = \frac{\sqrt{\pi}}{2\int_0^{\frac{\pi}{2}} \cos^{n-l-1}\varphi d\varphi}.$$

Recall that

$$\int \cos^n x dx = \frac{\cos^{n-1} x \sin x}{n} + \frac{n-1}{n}\int \cos^{n-2} x dx.$$

If n is even, when $l = 0$,

$$\int_0^{\frac{\pi}{2}} \cos^{n-1} x dx = \frac{n-2}{n-1}\cdot\frac{n-4}{n-3}\cdots\frac{2}{3}\int_0^{\frac{\pi}{2}} \cos x dx = \frac{n-2}{n-1}\cdot\frac{n-4}{n-3}\cdots\frac{4}{5}\cdot\frac{2}{3};$$

for $l = 1$,

$$\int_0^{\frac{\pi}{2}} \cos^{n-2} x dx = \frac{n-3}{n-2}\cdot\frac{n-5}{n-4}\cdots\frac{1}{2}\int_0^{\frac{\pi}{2}} \cos^0 x dx = \frac{n-3}{n-2}\cdot\frac{n-5}{n-4}\cdots\frac{3}{4}\cdot\frac{1}{2}\cdot\frac{\pi}{2}.$$

Implies that

$$\int_0^{\frac{\pi}{2}} \cos^{n-1} x dx \times \int_0^{\frac{\pi}{2}} \cos^{n-2} x dx = \frac{1}{n-1}\cdot\frac{\pi}{2}.$$

Therefore,

$$\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+1}{2})}{\Gamma(\frac{n}{2})} \times \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1+1}{2})}{\Gamma(\frac{n-1}{2})} = \frac{2}{n-1}\frac{\pi}{4\cdot\frac{1}{n-1}\cdot\frac{\pi}{2}} = 1.$$

The same results hold when n is odd.
By Lemma 1,

$$\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+1}{2})}{\Gamma(\frac{n}{2})} > \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1+1}{2})}{\Gamma(\frac{n-1}{2})},$$

hence,

$$\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+1}{2})}{\Gamma(\frac{n}{2})} > 1 > \sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1+1}{2})}{\Gamma(\frac{n-1}{2})}.$$

Lemma 6 *For given* C''_{pk} *and* σ

(a) When $T \leq M$,

$$\mu = \begin{cases} LSL + 3\sigma C''_{pk} & if\ \mu \leq T \\ USL - 3\sigma C''_{pk}\frac{D_u}{D_l} & if\ \mu \geq T \end{cases}$$

(b) when $T \geq M$,

$$\mu = \begin{cases} LSL + 3\sigma C''_{pk}\frac{D_l}{D_u} & if\ \mu \leq T \\ USL - 3\sigma C''_{pk} & if\ \mu \geq T \end{cases}$$

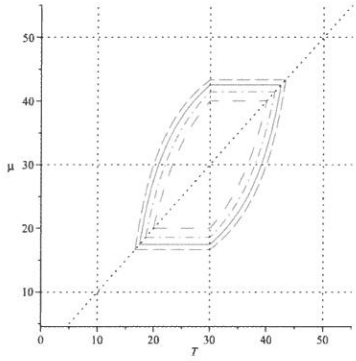

Figure 1. $C''_{pk} = 1.0$ and dash:$\sigma = 2.22$, solid:$\sigma = 2.49$, dashdot:$\sigma = 2.86$, spacedash:$\sigma = 3.33$

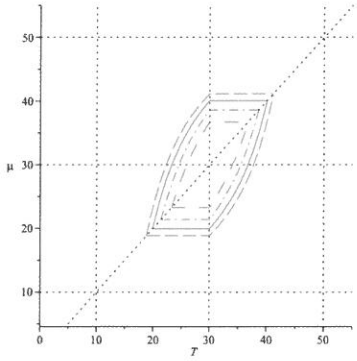

Figure 2. $C''_{pk} = 1.33$ and dash:$\sigma = 2.22$, solid:$\sigma = 2.49$, dashdot:$\sigma = 2.86$, spacedash:$\sigma = 3.33$

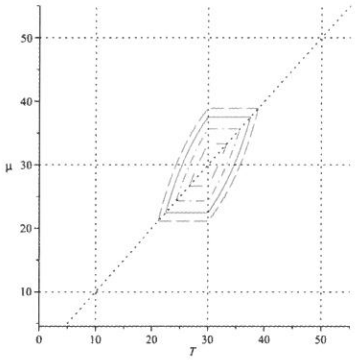

Figure 3. $C''_{pk} = 1.67$ and dash:$\sigma = 2.22$, solid:$\sigma = 2.49$, dashdot:$\sigma = 2.86$, spacedash:$\sigma = 3.33$

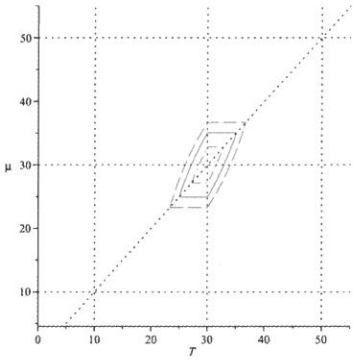

Figure 4. $C''_{pk} = 2.0$ and dash:$\sigma = 2.22$, solid:$\sigma = 2.49$, dashdot:$\sigma = 2.86$, spacedash:$\sigma = 3.33$

Table 1: Definion and MSEs for estimatiors of C_p

	Definition	MSE
$\widehat{C_p}$	$\frac{K}{S}$	$K^2\theta^2\left(\frac{2n-4}{n-3}-\frac{2}{A_{(n)}}\right)$
$\widehat{C_p^U}$	$A_{(n)}\frac{K}{S}$	$K^2\theta^2\left(C_{(n)}-1\right)$
$\widehat{C_p^M}$	$B_{(n)}\frac{K}{S}$	$K^2\theta^2\left(1-C_{(n)}^{-1}\right)$
$\widehat{C_p^S}$	$Kv\theta_0(1-W'_{(n,u)})+K\frac{A_{(n)}}{S}W'_{(n,u)}$	$K^2\theta^2\left((v\Delta-1)^2(1-W'_{(n,u)})^2+W'^2_{(n,u)}(C_{(n)}^{-1}-1)\right)$
$\widehat{C_p^{B1}}$	$\frac{K}{S}\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n+c-1}{2})}{\Gamma(\frac{n+c-2}{2})}$	$K^2\theta^2\left(\frac{2\Gamma[(n+c-1)/2]}{\Gamma[(n+c-2)/2]}\left\{\frac{\Gamma[(n+c-1)/2]}{(n-3)\Gamma[(n+c-2)/2]}-\frac{\Gamma[(n-2)/2]}{\Gamma[(n-1)/2]}\right\}+1\right)$
$\widehat{C_p^{B2}}$	$\frac{K}{S}\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-d+1}{2})}{\Gamma(\frac{n-d}{2})}$	$K^2\theta^2\left(\frac{2\Gamma[(n-d+1)/2]}{\Gamma[(n-d)/2]}\left\{\frac{\Gamma[(n-d+1)/2]}{(n-3)\Gamma[(n-d)/2]}-\frac{\Gamma[(n-2)/2]}{\Gamma[(n-1)/2]}\right\}+1\right)$

where

$$A_{(n)}=\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-1}{2})}{\Gamma(\frac{n-2}{2})},\quad B_{(n)}=\sqrt{\frac{2}{n-1}}\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-3}{2})},\quad C_{(n)}=\frac{\Gamma(\frac{n-1}{2})\Gamma(\frac{n-3}{2})}{\Gamma^2(\frac{n-2}{2})},\quad K=\frac{USL-LSL}{6},$$

$$W'_{(n,u)}=\left(\frac{\Gamma(\frac{n-2}{2})}{\Gamma(\frac{n-1}{2})}\right)^u\left(\frac{\Gamma(\frac{n-u-1}{2})}{\Gamma(\frac{n-2u-1}{2})}\right),\theta=\frac{1}{\sigma}\quad\Delta=\frac{\theta_0}{\theta},\quad c\geq 0,\quad d\geq 0,\quad u\neq 0,\quad v>0,$$

θ_0 is a guessed value of θ and available in addition to sample information.

Table 2: Proportion of estimators which perform the best out of 32 different combinations when $T = \mu$

n	MSE	MSE u=-1	MSE u=1	$\lvert BIAS \rvert$	$\lvert BIAS \rvert$ u=-1	$\lvert BIAS \rvert$ u=1	SE u=-1,1
6	3: 32	3: 1 4: 31	3: 0 4: 32	2: 24 6(1): 8	2: 20 6(1): 6 4: 6	2: 19 6(1): 6 4: 7	6(5): 32
10	3: 8 2: 24	3: 0 2: 6 4: 26	3: 0 2: 4 4: 28	6(1): 32	6(1): 28 4: 4	6(1): 28 4: 4	6(5): 32
30	2: 24 6(1): 8	2: 6 6(1): 4 4: 22	2: 4 6(1): 4 4: 24	6(1): 10 1: 18 5(2): 4	6(1): 10 1: 18 5(2): 4 4: 0	6(1): 10 1: 18 5(2):4 4: 0	6(5): 32
70	6(1): 22 1: 8 5(2): 2	6(1): 6 1: 4 5(2): 1 4: 21	6(1): 6 1: 4 5(2) :1 4: 21	1: 4 5(2): 20 5(3): 8	1: 4 5(2): 20 5(3): 8 4: 0	1: 4 5(2): 20 5(3): 8 4: 0	6(5): 32
100	6(1): 6 1: 16 5(2): 10	6(1): 0 1: 6 5(2): 5 4: 21	6(1): 0 1: 6 5(2): 5 4: 21	5(2): 12 5(3): 18 5(4): 2	5(2): 12 5(3): 17 5(4): 2 4: 1	5(2): 12 5(3): 17 5(4): 2 4: 1	6(5): 32
300	5(2): 2 5(3): 12 5(4): 12 5(5): 6	5(2): 0 5(3): 1 5(4): 7 5(5): 3 4: 21	5(2): 0 5(3): 1 5(4): 7 5(5): 3 4: 21	5(3): 2 5(4): 12 5(5): 18	5(3): 1 5(4): 11 5(5): 14 4: 6	5(3): 1 5(4): 11 5(5): 14 4: 6	6(5): 32
500	5(3): 2 5(4): 8 5(5): 22	5(3): 0 5(4): 0 5(5): 11 4: 21	5(3): 0 5(4): 0 5(5): 11 4: 21	5(4): 2 5(5): 30	5(4): 1 5(5): 16 4: 15	5(4): 1 5(5): 16 4: 15	6(5): 32
1000	5(5): 32	5(5): 0 4: 32	5(5): 0 4: 32	5(5): 32	5(5): 0 4: 32	5(5): 0 4: 32	6(5): 32

Table 3: Proportion of estimators which perform the best out of 468 different combinations when $T \neq \mu$

n	C''_{pk}	MSE		MSE $u=-1$		MSE $u=1$		$\lvert BIAS\rvert$	$\lvert BIAS\rvert$ u=-1,1	SE u=-1,1
		T<30	T>30	T<30	T>30	T<30	T>30			
6	1.0	3: 92	3: 92	3: 86 4: 6	3: 47 4: 45	3: 78 4: 14	3: 43 4: 49	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 45 4: 25	3: 20 4: 50	3: 35 4: 35	3: 14 4: 56			
	1.67	3: 46	3: 46	3: 0 4: 46	3: 0 4: 46	3: 0 4: 46	3: 0 4: 46			
	2.0	3: 26	3: 26	3: 0 4: 26	3: 0 4: 26	3: 0 4: 26	3: 0 4: 26			
		3: 468		3: 198	4: 270	3: 170	4: 298			
10	1.0	3: 92	3: 92	3: 92 4: 0	3: 57 4: 35	3: 32 4: 61	3: 9 4: 83	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 64 4: 6	3: 37 4: 33	3: 56 4: 14	3: 27 4: 43			
	1.67	3: 46	3: 46	3: 18 4: 28	3: 8 4: 38	3: 16 4: 30	3: 8 4: 38			
	2.0	3: 26	3: 26	3: 0 4: 26	3: 0 4: 26	3: 0 4: 26	3: 0 4: 26			
		3: 468		3: 271	4: 197	3: 147	4: 321			
30	1.0	3: 92	3: 92	3: 92 4: 0	3: 65 4: 27	3: 23 4: 69	3: 10 4: 82	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 70 4: 0	3: 40 4: 30	3: 29 4: 41	3: 19 4: 51			
	1.67	3: 46	3: 46	3: 36 4: 10	3: 16 4: 30	3: 1 4: 45	3: 0 4: 46			
	2.0	3: 26	3: 26	3: 0 4: 26	3: 0 4: 26	3: 0 4: 26	3: 0 4: 26			
		3: 468		3: 319	4: 149	3: 92	4: 376			
70	1.0	3: 92	3: 92	3: 92 4: 0	3: 66 4: 26	3: 82 4: 10	3: 54 4: 38	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 70 4: 0	3: 44 4: 26	3: 55 4: 15	3: 34 4: 36			
	1.67	3: 46	3: 46	3: 40 4: 6	3: 18 4: 28	3: 41 4: 5	3: 22 4: 24			
	2.0	3: 26	3: 26	3: 0 4: 26	3: 0 4: 26	3: 8 4: 18	3: 2 4: 24			
		3: 468		3: 334	4: 134	3: 298	4: 170			

Table 3(continuous)

n	C''_{pk}	MSE		MSE $u=-1$		MSE $u=1$		$\lvert BIAS\rvert$	$\lvert BIAS\rvert$ u=-1,1	SE u=-1,1
		T<30	T>30	T<30	T>30	T<30	T>30			
100	1.0	3: 92	3: 92	3: 92 4: 0	3: 67 4: 25	3: 39 4: 53	3: 52 4: 40	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 70 4: 0	3: 44 4: 26	3: 46 4: 24	3: 30 4: 40			
	1.67	3: 46	3: 46	3: 40 4: 6	3: 20 4: 26	3: 39 4: 7	3: 18 4: 28			
	2.0	3: 26	3: 26	3: 0 4: 26	3: 2 4: 24	3: 6 4: 20	3: 2 4: 24			
		3: 468		3: 337	4: 131	3: 232	4: 236			
300	1.0	3: 92	3: 92	3: 90 4: 0	3: 68 4: 24	3: 56 4: 36	3: 50 4: 42	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 70 4: 0	3: 44 4: 26	3: 70 4: 0	3: 49 4: 21			
	1.67	3: 46	3: 46	3: 40 4: 6	3: 21 4: 25	3: 0 4: 46	3: 0 4: 46			
	2.0	3: 26	3: 26	3: 5 4: 21	3: 2 4: 24	3: 1 4: 25	3: 0 4: 26			
		3: 468		3: 342	4: 126	3: 226	4: 242			
500	1.0	3: 92	3: 92	3: 92 4: 0	3: 68 4: 24	3: 92 4: 0	3: 76 4: 16	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 70 4: 0	3: 44 4: 26	3: 70 4: 0	3: 49 4: 21			
	1.67	3: 46	3: 46	3: 40 4: 6	3: 22 4: 24	3: 39 4: 7	3: 20 4: 26			
	2.0	3: 26	3: 26	3: 6 4: 20	3: 2 4: 24	3: 10 4: 16	3: 0 4: 23			
		3: 468		3: 344	4: 124	3: 359	4: 109			
1000	1.0	3: 92	3: 92	3: 92 4: 0	3: 68 4: 24	3: 83 4: 9	3: 69 4: 23	2: 468	2: 468	6(5): 468
	1.33	3: 70	3: 70	3: 70 4: 0	3: 44 4: 26	3: 6 4: 64	3: 6 4: 64			
	1.67	3: 46	3: 46	3: 40 4: 6	3: 22 4: 24	3: 43 4: 3	3: 24 4: 22			
	2.0	3: 26	3: 26	3: 6 4: 20	3: 2 4: 24	3: 10 4: 16	3: 4 4: 22			
		3: 468		3: 344	4: 124	3: 245	4: 223			

Table 4: Proportion of estimators which perform the best out of 32 different combinations when $T \neq \mu$ and $T = M$

n		C_{pk}''	MSE	MSE u=-1	MSE u=1	$\lvert BIAS \rvert$	$\lvert BIAS \rvert$ u=-1,1	SE u=-1,1
6	$\lvert T-\mu \rvert > 0.02$	1	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 0 4: 8	3: 0 4: 8	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 0 4: 6	3: 0 4: 6	2: 6	2: 6	6(5): 6
	$\lvert T-\mu \rvert \leq 0.02$	2.0	3: 2	3: 0 4: 2	3: 0 4: 2	2: 2	2: 2	6(5): 2
10	$\lvert T-\mu \rvert > 0.02$	1	3: 8	3: 8 4: 0	3: 0 4: 8	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 6 4: 2	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 0 4: 6	3: 0 4: 6	2: 6	2: 6	6(5): 6
	$\lvert T-\mu \rvert \leq 0.02$	2.0	2: 2	2: 0 4: 2	2: 0 4: 2	6(1): 2	6(1): 2	6(5): 2
30	$\lvert T-\mu \rvert > 0.02$	1	3: 8	3: 8 4: 0	3: 0 4: 8	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 5 4: 3	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 0 4: 8	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 0 4: 6	3: 0 4: 6	2: 6	2: 6	6(5): 6
	$\lvert T-\mu \rvert \leq 0.02$	2.0	2: 2	2: 2 4: 0	2: 0 4: 2	1: 2	1: 2	6(5): 2
70	$\lvert T-\mu \rvert > 0.02$	1	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 3 4: 5	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 6 4: 0	3: 6 4: 0	2: 6	2: 6	6(5): 6
	$\lvert T-\mu \rvert \leq 0.02$	2.0	6(1): 2	6(1): 2 4: 0	6(1): 2 4: 0	5(2): 2	5(2): 2	6(5): 2

Table 4 (continuous)

n		C''_{pk}	MSE	MSE u=-1	MSE u=1	$\|BIAS\|$	$\|BIAS\|$ u=-1,1	SE u=-1,1
100	$\|T-\mu\| > 0.02$	1	3: 8	3: 8 4: 0	3: 3 4: 5	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 7 4: 1	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 6 4: 0	3: 5 4: 1	2: 6	2: 6	6(5): 6
	$\|T-\mu\| \leq 0.02$	2.0	1: 2	1: 2 4: 0	1: 2 4: 0	5(2): 2	5(2): 2	6(5): 2
300	$\|T-\mu\| > 0.02$	1	3: 8	3: 8 4: 0	3: 3 4: 5	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 0 4: 8	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 6 4: 0	3: 0 4: 6	2: 6	2: 6	6(5): 6
	$\|T-\mu\| \leq 0.02$	2.0	5(3): 2	5(3): 2 4: 0	5(3): 2 4: 0	5(4): 2	5(4): 2	6(5): 2
500	$\|T-\mu\| > 0.02$	1	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 7 4: 1	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 6 4: 0	3: 6 4: 0	2: 6	2: 6	6(5): 6
	$\|T-\mu\| \leq 0.02$	2.0	5(4): 2	5(4): 2 4: 0	5(4): 2 4: 0	5(5): 2	5(5): 2	6(5): 2
1000	$\|T-\mu\| > 0.02$	1	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.33	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		1.67	3: 8	3: 8 4: 0	3: 8 4: 0	2: 8	2: 8	6(5): 8
		2.0	3: 6	3: 6 4: 0	3: 6 4: 0	2: 6	2: 6	6(5): 6
	$\|T-\mu\| \leq 0.02$	2.0	5(5): 2	5(5): 2 4: 0	5(5): 2 4: 0	5(5): 2	5(5): 0 4: 2	6(5): 2

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製程能力指標 C''_{pk} 估計式之比較研究

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摘 要

對於一個具有非對稱公差之製程 Pearn 及 Chen 在 1998 年提出一個廣義的製程能力指標 C''_{pk}，在該文中作者提供指標之最大概似估計式。在常態製程的前提下，本文根據 Singh and Saxena(2005) 一文之結論另外提供了六個 C''_{pk} 之間接估計式。透過數值方式之比較，我們得知本文所提供之間接估計式最在很多情況下優於最大概似估計式。

關鍵字：間接估計式；近似不偏性；一致估計式。

高速互補金氧半影像感應器類比前端電路之設計與製作

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摘　要

隨著數位相機的日漸普及，人人隨手一台就可以紀綠影像及聲音，加上多功能事務機的出現，更讓一般掃描文件變得簡單。影像處理 IC 已經和社會大眾所能接受的消費性電子產品密不可分。在設計影像處理 IC 的核心電路，一直以來都是由二大架構在彼此競爭，一是由標準的 CMOS 架構所組成，而另外一種是由 CCD 架構所組成。

目前此二大架構之產品應該主要是以價格及解析度來做為區分。因為 CCD 架構的影像處理 IC，具有 S/N 佳及動態範圍大之優點，所以主要是被應用在高解析度及快掃描速度為主之影像產品。反之，CMOS 架構之影像處理 IC，因 S/N 不如 CCD 架構且由於電路所包含之 offset 需要做處理，所以被應用在低解析度及掃描速度慢之產品。

本論文旨在於探討 CMOS 及 CCD 技術下之影像感測器架構。並針對 CMOS 影像 IC 在設計類比前端讀取電路時，需考慮的設計規格而提出一種不同於一般傳統 CMOS 類比前端讀取電路之架構來克服 S/N 不如 CCD 架構之問題，進而使此架構能被應用在更高解析度及快掃描速度上。

1. 前　言

影像在可見光光譜範圍內的應用技術，主要有二種且皆是由矽材質所構成影像感測器，分別為電荷耦合式元件(Charge Couple Device, CCD)和CMOS影像感測器(CMOS Image Sensor)。儘管兩者皆是以相同的矽當成基底在使用，但是在吸收光子的特性及操作方式還是有相當大的差別。CCD 會被使用這麼多年至今，主要是由於它的極小暗電流特性，非常高的光子轉移效率，低的固定樣本雜訊 (Fixed Pattern Noise, FPN)，和小的像素尺寸。然而在最近的十幾年中，CMOS 影像感測器的快速崛起更是因為其低功率消耗的特性，低的晶片製作成本及容易和 VLSI 電路整合在同一晶片上之優點。多數市面上的消費性影像類的產品是由 CMOS 影像感測器所構成。

整個影像感測架構包含四大部份，分別為一光感測器，類比前端讀取電路，後段的類比轉數位信號處理方塊和影像輸出裝置。其中光感測器較常被使用的如早期的 CCD 到最近幾年的 CMOS 影像感測器。而類比前端讀取電路則因為前者種類及訊號處理方式的不同而有相當大的差異。

在所有的光譜領域中，從極短波長 (α 或 γ 射線) 到超長波長 (遠紅外線或微波)，其中較為一般大眾所熟知的是可見光領域，波長從 400nm 到 700nm，如圖 1 所示。然而，由矽元件所構成的光感測器如電荷耦合式元件 (CCD) 及 CMOS 影像感測器在可見光領域的轉移效率最佳，也最適合被拿來做為商業化的產品。本論文集中在可見光領域中的 CCD 和 CMOS 這二類，而其發展過程如圖 2 所示，較詳細的內容可以參考文獻 [7]。

在 1966 年時，Westinghouse 首先提出由光電晶體 (Photo BJT) 組成的 50 $\times$ 50 陣列架構的黑白感測器 [1]，其中因為這些光感測器並沒有被電路做放大，所以靈敏度 (Sensitivity) 很低，所以在這感測器的後端需要接一個放大器來處理訊號。在 1968 年，一個由光二極體 (Photo Diode) 所組成 100 $\times$ 100 的陣列式感測器，採用 APS 架構已被提出 [2]。在 1970 年，電荷耦合式的裝置 (Charge Couple Device, CCD) 第一次被提出 [3]，最受到注目的是其極低的固定樣本雜訊 (Fixed Pattern Noise, FPN)，從此之後的 10 年在光感測器應用幾乎都是以 CCD 為主，一直到 1980 年後，改良的 CMOS 才再度被發展出來。

在 1990 年前期，由英國愛丁堡大學 VVL(VLSI Vision Ltd) 提出 PPS 架構的影像晶片 [4]，也因此種 PPS 的架構只適合應用在中小型的陣列式且操作在中低速度的影像感測晶片。1992 年美國太空總署 JPL 開始研究如何讓 APS 架構的光感測器能得到低的雜訊 [5]，到了 1995 年低雜訊的 CMOS APS 被成功地整合在一 VLSI 晶片裡，並具有低

功率消耗，低製造成本，且能抗幅射干擾之優點。從此以後，由 CMOS 影像感測器所發展成的電子消費性產品就非常受到歡迎，包含電腦用的攝影機 (PC Camera)，照相式手機 (Cellular Phone Cameras)，個人數位幫手 (PDA) 等。

儘管 1970 到 1980 年代，CCD 是在影像感測領域中的主流技術，甚至到現在的攝影機，多數也是由 CCD 感測器做成的。最主要原因是影像品質上，CCD 還是比 CMOS 勝過很多。而 CMOS 影像感測器做成的產品，仍然以低耗能且可攜帶式的消費性產品為主。

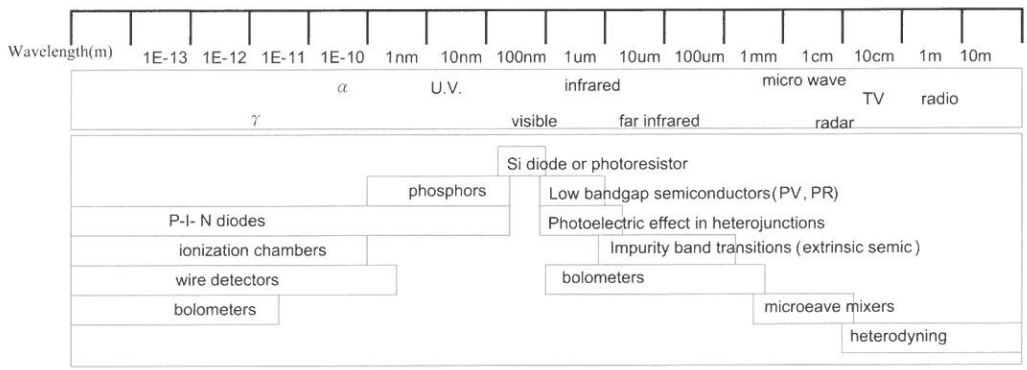

圖 1 感測器在不同光波長的應用

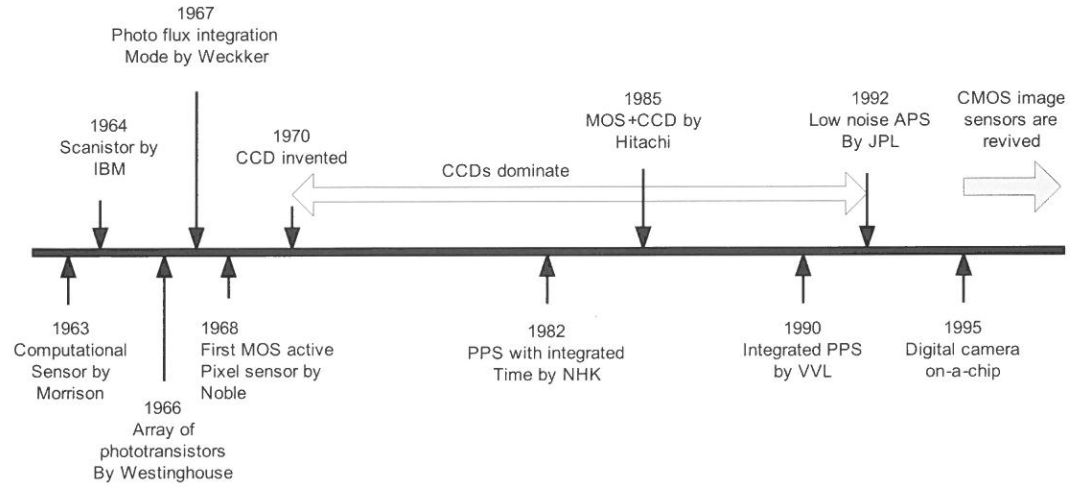

圖 2 CCD 和 CMOS 的發展過程圖

如圖 3 所示，CCD 影像感測器之操作主要是以電荷傳輸為主，可以細分成四個動作來完成，分別是光電轉換、儲存訊號、訊號傳輸、訊號的檢測。將待測物在照光後轉換成相對應的訊號電荷，再把每個光電二極體所感應到的訊號電荷做儲存動作，之後將訊號電荷先做垂直方向傳輸，然後再做水平方向之傳輸，最後再把訊號電荷透過放大器轉成電壓訊號放大並讀取出來。

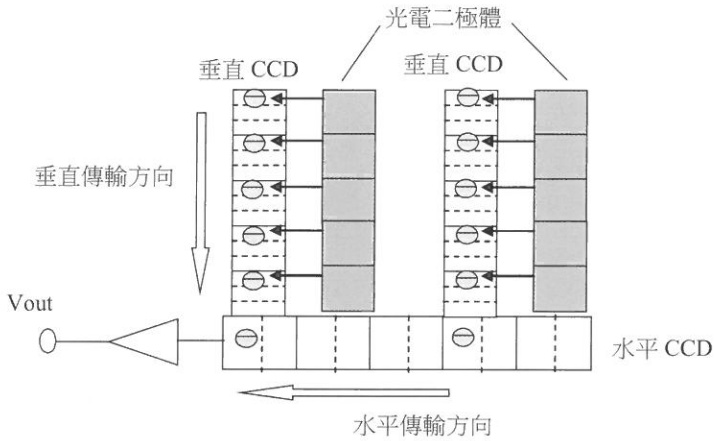

圖 3CCD 影像感測器之動作

相較於 CCD 的電荷傳輸，如圖 4 所示 CMOS 影像感測器之操作就是以電壓傳輸為主，傳輸動作一樣可以細分成四個動作來完成，分別是光電轉換、荷電轉換、儲存訊號、訊號傳遞。將待測物在照光後轉換成相對應到的訊號電荷，再把訊號電荷透過放大器直接轉成電壓訊號，之後儲存每個由光電二極體所相對應的電壓訊號，最後依垂直方向及水平方向把電壓訊號傳遞出來。

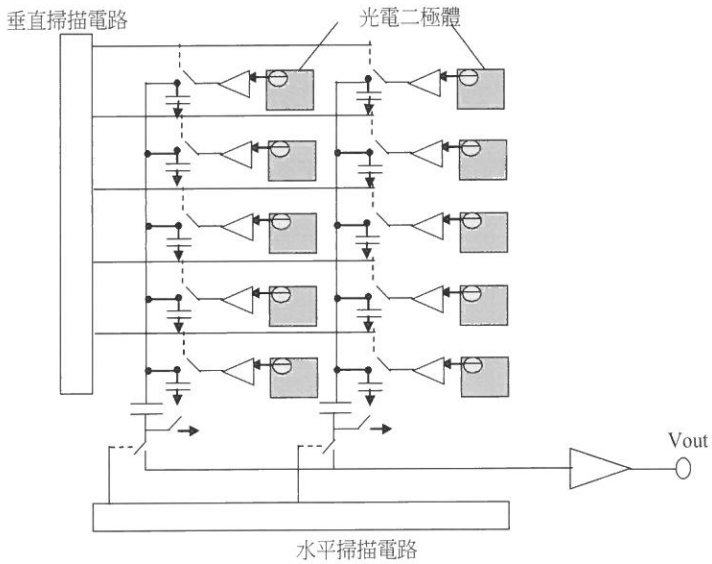

圖 4CMOS 影像感測器之動作

如圖 5 所示，在 CMOS 影像感測器的架構中，每一列的光二極體所累積的電荷會透過 MOS 開關傳至每一條 Bit line 至 Column 的電容裡儲存，接著再透過 Column 多工器來選擇訊號線並傳送至輸出端。

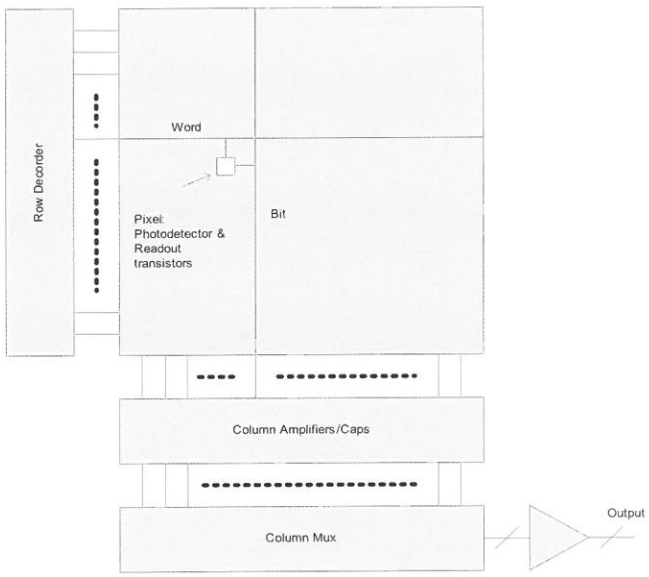

圖 5 CMOS 影像感測器的架構

如圖 6 所示，CMOS 影像感測器裡，像素的架構主要分成兩種，分別為 PPS 及 APS。PPS 架構裡，每一像素只有一個開關用的電晶體及光感測器，因此光感測器的 fill factor 很高，但是有很低的訊號雜訊比 (SNR)。在 APS 架構裡，每一個像素會有 3~4 個電晶體來組成一個簡單的放大器及單一開關，因而讀取速度快，缺點是光感測器的 fill factor 會比較低。當然，在使用 0.5 m 以下的製程時，fill factor 會被大大的提高也變得不再是 APS 的缺點了。

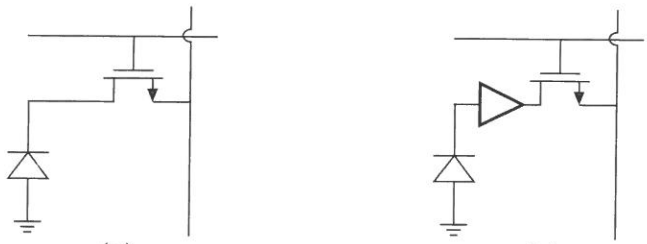

圖 6 CMOS 像素的架構 (a) PPS 架構 (b) APS 架構

由 PPS 架構所組成的 CMOS 影像感測器，如圖 7 所示在 Column 的方塊圖裡，除了每一像素分別連接到不同的 Bit line 及 Word line 外，在 Column 的方塊圖裡有一電荷轉電壓的放大器及一電容，其中電容被用來儲存從每列像素所傳遞過來的電荷並轉成電壓的訊號值，最後就透過 Column 多工器來分別把訊號由放大器傳出。

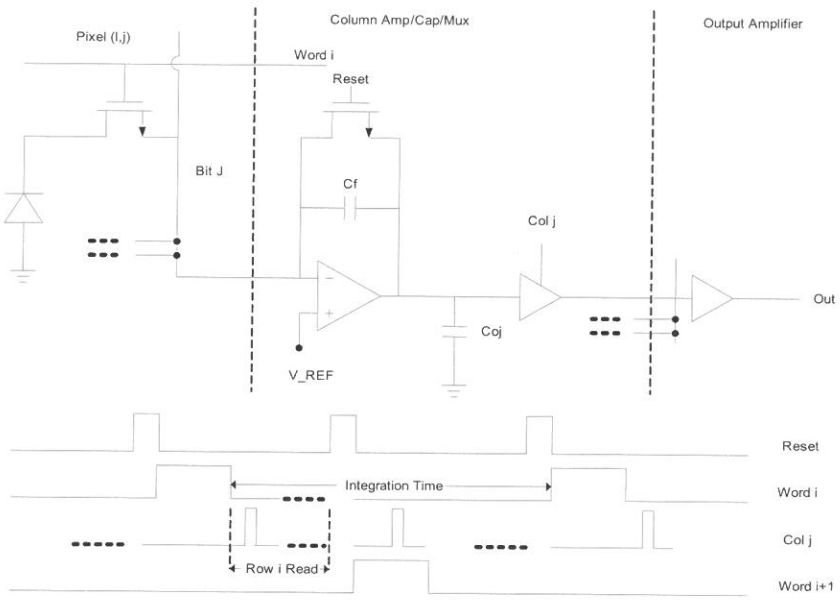

圖 7 CMOS PPS 架構及時序圖 -1

整個 PPS 的動作，是把每個像素內的電荷，透過 Column 裡電荷放大器轉成電壓後再由後端的二級 Source Follower 放大器傳至輸出端，如圖 8 所示。這種讀取電荷的方式是屬於破壞式的讀取，CCD 的也是屬於這種方式。另外，每個像素裡的光二極體的二端點偏壓，在讀取週期時均會被控制在 VREF 到地的逆向偏壓位準，這個特性是因為 Column 裡的電荷放大器所造成的。

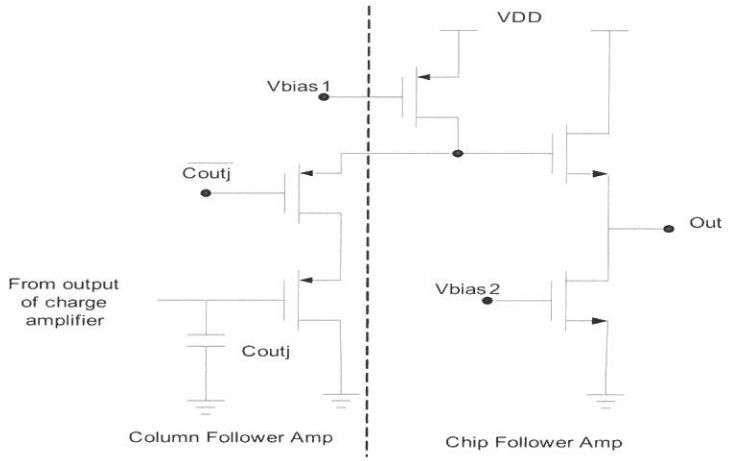

圖 8 CMOS PPS 架構的列輸出放大

如圖 9 所示，PPS 的影像感測器能被精簡。在穩定的狀態時，假設電荷 Q 被光二極體累積直到累積週期結束時，輸出電壓 $v_o = VREF + Q / C_f$，而這也代表 PPS 的轉換增益為 Q / C_f。當 $Q = 0$ 時，在忽略暗電流特性時，可以得到 $v_{o(\max)} = VREF$; 然而輸出電壓的最大值是發生在光二極體的陰極端為地時，最大的輸出電壓 $v_{o(\max)} = VREF + (C_D / C_f) \times VREF$。

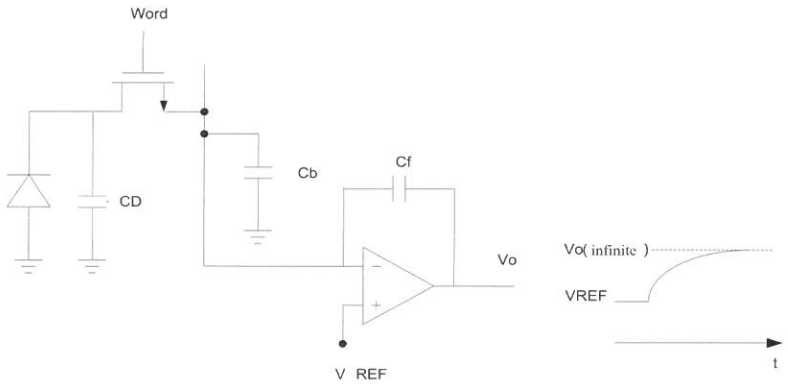

圖 9 PPS 電荷至輸出電壓轉移圖

有一件很重要的事情，就是輸出電壓的最大值不可以超過放大器的最大值，不然會有訊號被放大器卡掉的問題出現。所以整個 PPS 能輸出的範圍是從 *VREF* 到 $(C_D / C_f) \times VREF$。

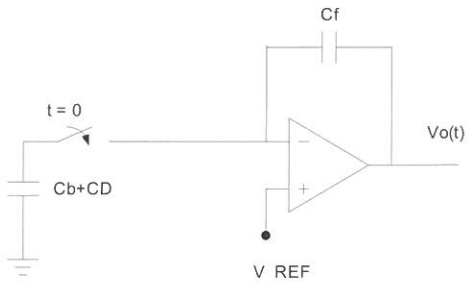

圖 10 PPS 讀取週期等效圖

PPS 的讀取週期分成二個階段，一是從每一列像素到 Column 電容，二是 Column 解碼器 / 多工器被使用來把一個個在像素裡的資料被串列式的讀出。因此，從列到行的轉移時間會是關鍵。讀取週期的模型如圖 10 所示，在使用 Single Pole 的放大器模型且假設開關電阻是零來分析，在電荷放大器的輸入和輸出端的關係為

$$\frac{Vo(s)}{V_+(s)-V_-(s)} = A(s) = \frac{A}{1+\left(\frac{s}{\omega_0}\right)} \tag{1}$$

讀取電路可以被假設成如圖 11 所示的模型，進而得到

$$\frac{Vo(s)}{Vi(s)} \approx \frac{C_b + C_D}{C_f} \times \frac{1}{1+\frac{s}{\frac{A\omega_0 C_f}{(C_b + C_D + C_f)}}} \tag{2}$$

而時間常數 $\tau = \dfrac{C_b + C_D + C_f}{A\omega_0 C_f}$ 。

若是考慮一個 256 × 256 的 PPS，$C_D = C_f = 20\text{fF}$，電荷放大器的 DC gain，$A = 6 \times 10^4$ 且 3dB 頻寬 $\omega_0 = 100\text{rad/s}$，經由上面公式可以得到時間常數為 5.88μs。$C_b$ 的大小會直接影響列傳輸時間的長短，而當列的數目很大時，C_b 的值就不會太小。再者若是放大器的頻寬能被設計到最大也能縮短列傳輸時間，只是會付出功率高的代價。

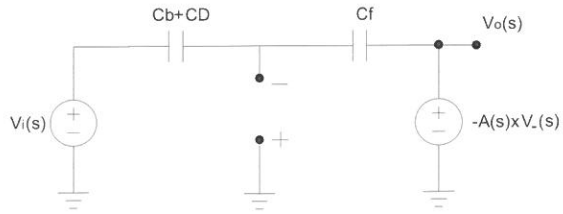

圖 11 PPS 讀取週期模型

在 CMOS 影像感測器另一種主動式的架構如圖 12 所示，相對於 PPS 的架構，在每一個像素裡多了由兩顆電晶體連接到 Bit line，及 Column 的放大器的電流源組成源極放大器 (Source Follower) 來取代在 PPS 架構裡的電荷放大器。

APS 架構的特點就是從每一個像素被讀出時就是電壓訊號，並不需要額外的轉換。再者光二極體和 Column 電容中間隔著源極放大器，所以訊號不是被破壞性讀出，且讀取速度也會因此而加快。每一列的訊號在被讀出後，光二極體所接的 NMOS 電晶體會把累積的電荷做清除動作，此時在陰極端上的電壓 $v_D = V_{DD}$-V_{TR}，這裡的 V_{TR} 指的是清除用的 NMOS 電晶體的 Threshold Voltage(包含 Body Effect)。

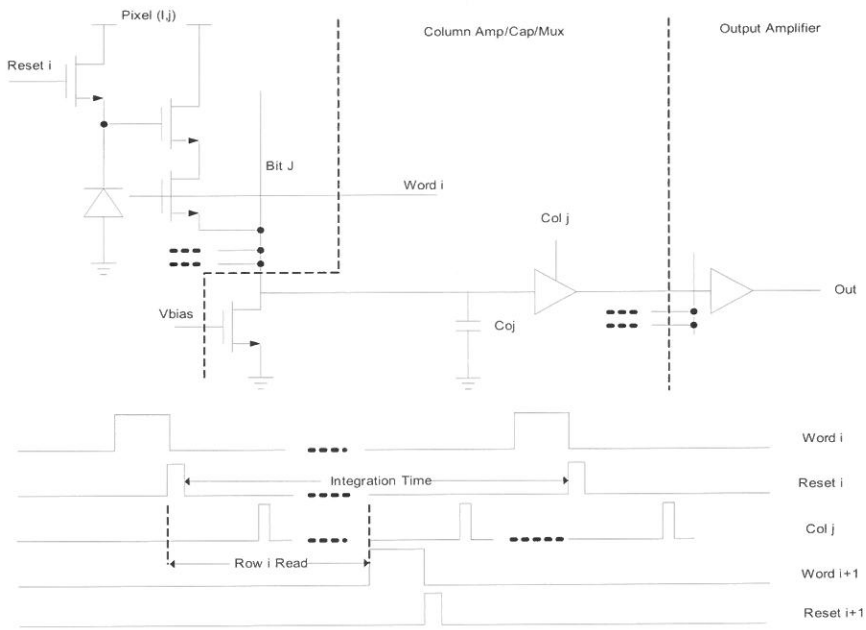

圖 12 CMOS PPS 架構及時序圖 -2

如圖 13 所示，APS 架構在穩定的狀況時，電荷 Q 被累積在光二極體的陰極端直到累積週期結束時，忽略在電晶體的壓降後，輸出電壓為

$$v_o = v_D - \frac{Q}{C_D} - v_{GSF} = (V_{DD} - V_{TR}) - \frac{Q}{C_D} - v_{GSF} \tag{3}$$

這裡的 v_{TR} 指的是清除用的 NMOS 的 Threshold Voltage(含 body effect)，而 vGSF 是源極放大器從閘極端到源極端的電壓差值，像素的轉換增益為 Q/C_D。輸出端的最小值為 $V_{o(min)} = V_{bias} - V_{TB}$。$V_{TB}$ 是閘極端接到 V_{bias} 的 NMOS 電晶體的 Threshold Voltage。然而輸出端的最大值發生在 Q = 0 時，$V_{o(max)} = V_{DD} - V_{TR} - v_{GSF}$

整個 APS 架構的輸出範圍 (Vs) 是由 $V_{o(max)}$ 減去 $V_{o(min)}$，最後得到

$$Vs = V_{DD} - V_{TR} - v_{GSF} - V_{bias} + V_{TB} \tag{4}$$

值得注意的是，Qmax = $V_D \times C_D$ 並不能完全被利用到，因為 $V_{o(min)}$ 會比光二極體的陰極電壓到地時先碰觸到，所以光二極體的最大值並沒有被全部有效的使用到。

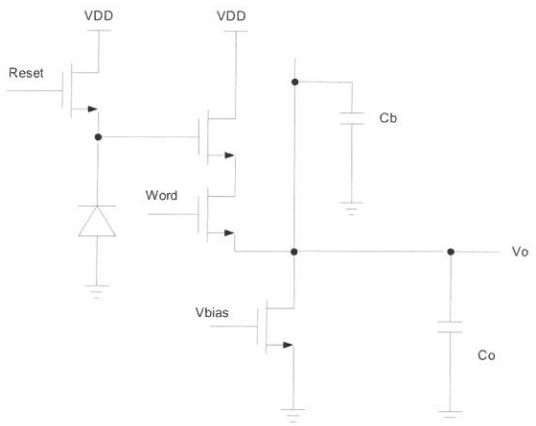

圖 13 CMOS APS 架構的列訊號放大

APS 架構的讀取時間是由每一列傳到 Column 電容的時間總合後再加上 Column 多工器到輸出端的傳遞時間，不同於 PPS 的是，APS 的 Column 讀取時間是真的由放大器的特性來決定，而不會跟每一列所貢獻的雜散電容有關。如圖 14 所示的等效圖，在一個 0.5μm 製程的 APS 感測器，有 256 列像素，$V_{TF} = 0.9V$，$V_{TR} = 1.1V$，$V_{TB} = 0.8V$，

$V_S = (V_{DD} - V_{TR} - v_{GSF}) - (V_{bias} - V_{TB}) = (3.3 - 1.1 - 1.0) - (1.0\text{-}0.8) = 1V$

$$1.88\times10^{-6} + C_0^{'}\cdot\frac{dv_0}{dt} = 188\times10^{-6}\times(1.3-v_0)^2$$

$$\int_0^{trow} dt = t_{row} = C_0^{'}\int_{0\,2}^{1.198}\frac{dv_0\times10^{-6}}{188(1.3-v_0)^2-1.88} = \frac{10^{-6}\times C_0^{'}}{188}\int_{0\,2}^{1.198}\frac{dv_0}{(1.3-v_0)^2-10^{-2}} = 444ns \tag{5}$$

比起 PPS 架構的 5.88 s，APS 的讀取時間快了十倍以上。

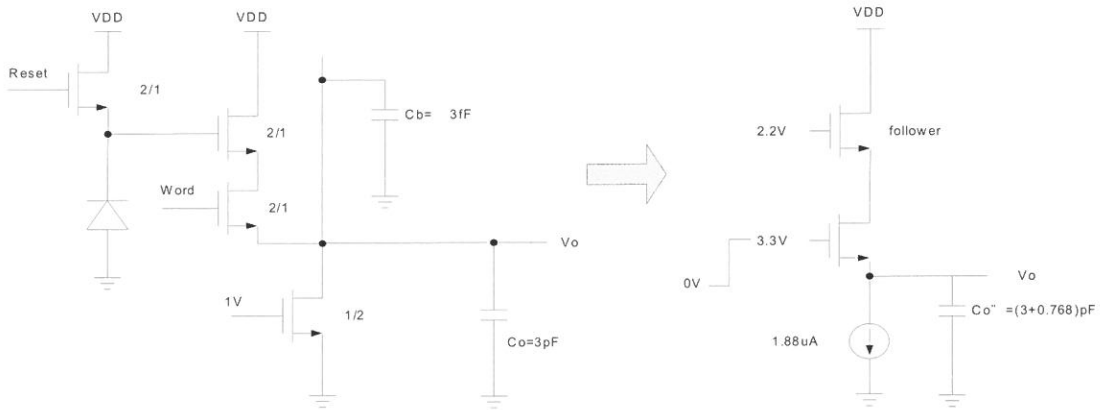

圖 14 CMOS APS 讀取週期等效圖

PPS 和 APS 在經過詳細的分析後，可以得到如表 1 所示的結果。

表 1 PPS 和 APS 比較

	PPS	APS
Fill Factor	> 80%	< 50%
Conversion Gain	Q/Cf	Q/CD
Charge Delievery	Destructive	Non-destructive
Readout Time	5.88us	444ns
Output Range	CD/Cf × VREF	VDD-VGSF-Vbias
	> 1.2V	~1.2V

最常被使用來當光感測器的是光二極體 [10]，在標準 CMOS 製程裡，有三種型式的光二極體可以使用，分別是 NWELL/PSUB，N+/PSUB，及 P+/NWELL。當然這三

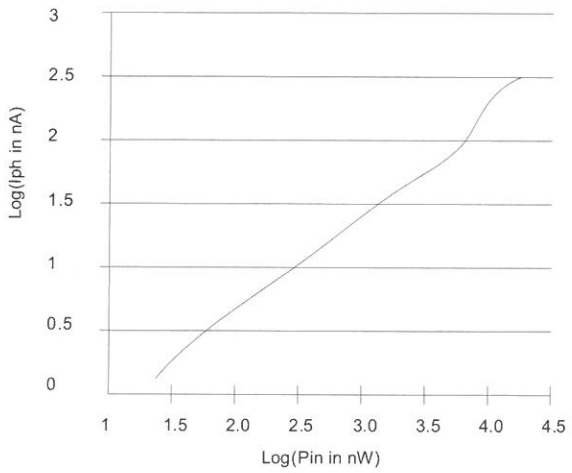

圖 17 100 μm × 100 μm Nwell/psub 之光電流量測

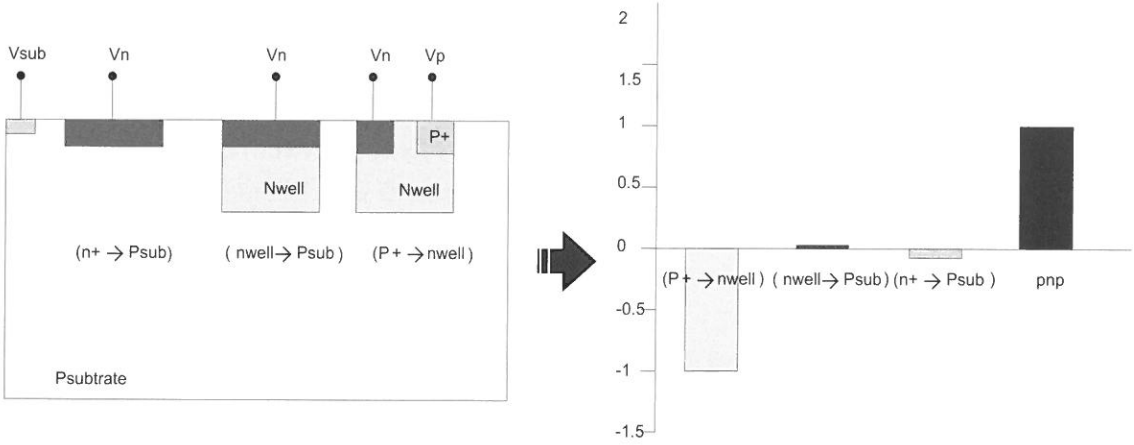

圖 18 PhotoBJT 和三種型式的 Photodiode 之光電流量測

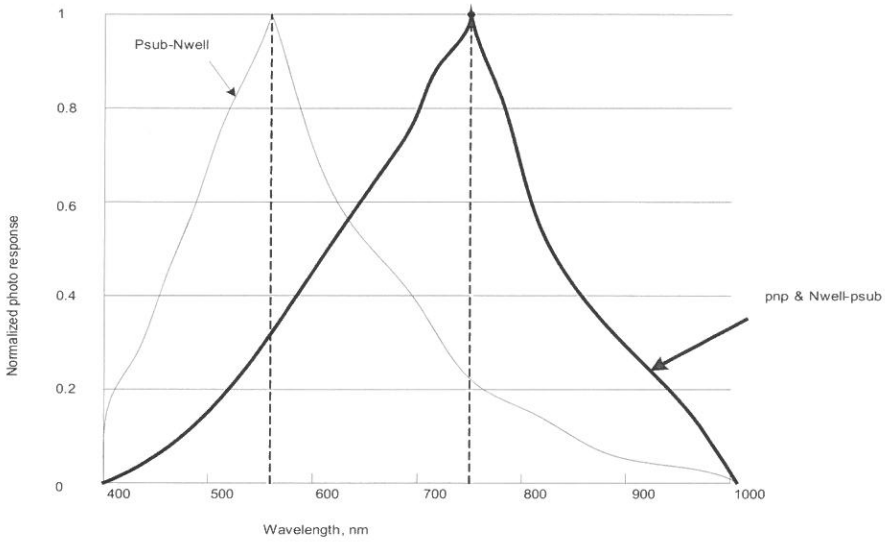

圖 19 PhotoBJT 和二種型式的 Photodiode 之光譜量測

2. 影像讀取電路之積體電路設計

基於上述的基本認知廣泛地探討 Photodiode 及 PhotoBJT 的特性，並做影像感測器應用層次上的電路模擬藉以評估其性能。在本論文中吾人使用積體電路製程技術加以影像感測器實作進而更準確分析電路的各項參數。常用的數位相機其構造如圖 20 所示，在影像感測器的後端是接著 AGC(Auto Gain Control) 和 ADC(Analog to Digital Converter)，透過 Auto Exposure 及 Auto Focus 分別來調整 Lens 光透鏡所引入的光強度和 AGC 來把影像感測器的訊號強度調至 ADC 所能反應的範圍，緊接著再由後端的數位訊號處理來做色彩的調整，包含了影像放大和補償，在這當中影像感測的飽合輸出電壓扮演著極為重要的角色。飽合輸出電壓定義為 $Vo_{sat} = Vo_{\max} - \mathrm{Vo}_{dark}$

具有大的飽合電壓的影像感測器能讓 AGC 使用較小的放大倍率就能把訊號傳送至 ADC，把光電訊號轉換成數位訊號。反之，若是影像感測器的飽合輸出電壓太小，就會讓 AGC 使用較大的放大倍率後傳至 ADC 處理，放大後的光電訊號品質會變差，原因是訊號被放大會連 Noise 也被放大了，這裡的 Noise 包含了 FPN 和光感測器上的暗電流。

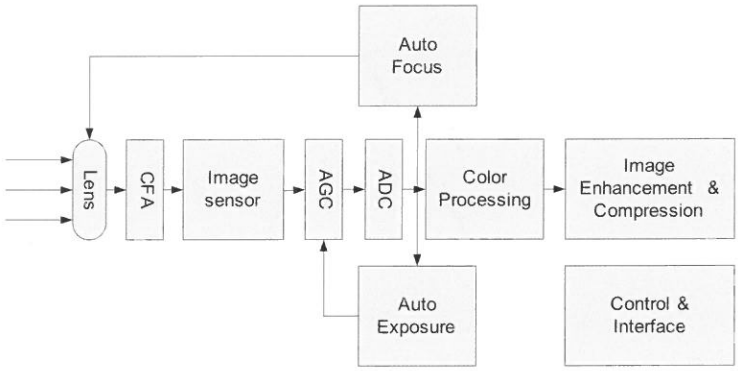

圖 20 Digital Camera 系統方塊圖

光感測器的暗電流指的是漏電流，這種電流不是被光子所激發所產生的，而是由光感測器兩端的逆向偏壓在 PN 介面上的漏電流。這個漏電流在經過長時間累積後，一樣會反應在感測器的輸出端，並減少原先飽合電壓的空間，讓真實的光電訊號能反應的範圍變小，如圖 21 所示。而 Vo_{max} 是感測器裡放大器的最大輸出電壓，一般由選定的放大器之架構來決定。

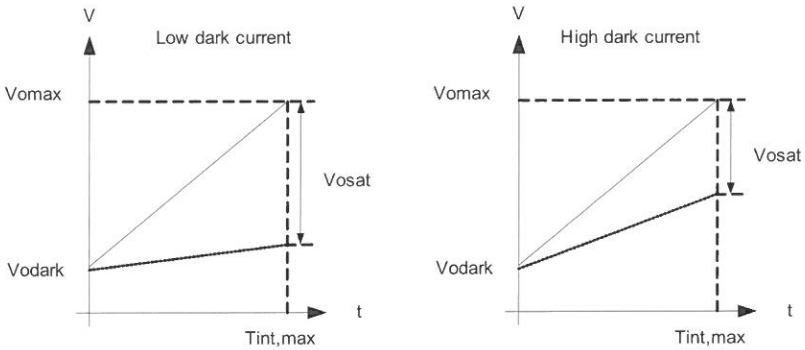

圖 21 飽合電壓和暗電流之關係

另外，一個重要的特性在評估光感測器的好壞是 S/N 比，定義 $S/N=20log(Vo_{(sat)}/V_{noise})$ V_{noise} 指的是影像感測器在不照光時，輸出端電壓的標準差。其公式如下

$$V_{std,noise} = \Delta Vo_{(darkcurrent)} + \Delta Vo_{(FPN)} + \Delta Vo_{(thermal)} \tag{10}$$

其中包含光感測器的暗電流大小和電路裡的 FPN 都會影響 V_{noise} 大小。這裡 $\Delta Vo_{(thermal)}$

指的是當溫度變化時，在不考慮光感測器時輸出端的 DC 位準的變化。好的 CMOS 影像感測器其 S/N 通常介於 40~50dB，而 CCD 的 S/N 比一般都至少 60dB 以上。本論文所探討的感測器之 S/N 比雖然不能媲美 CCD 的 60dB，但是也能達到約 50dB 左右的表現。

為了方便分析影像讀取電路之架構及動作原理，吾人均以一維的 CMOS 影像感測器為主。如果說多數在數位相機及 PC Camera 裡所使用的是陣列式的影像感測器，就是屬於二維的架構，而所謂一維的影像感測器是只採用二維架構裡的一列，如圖 22 所示。這種一維架構的影像感測器由於像素較少和單一個 Column 電路所以也較容易設計，目前這種一維的架構適合用在如條碼辨識器、傳真機。

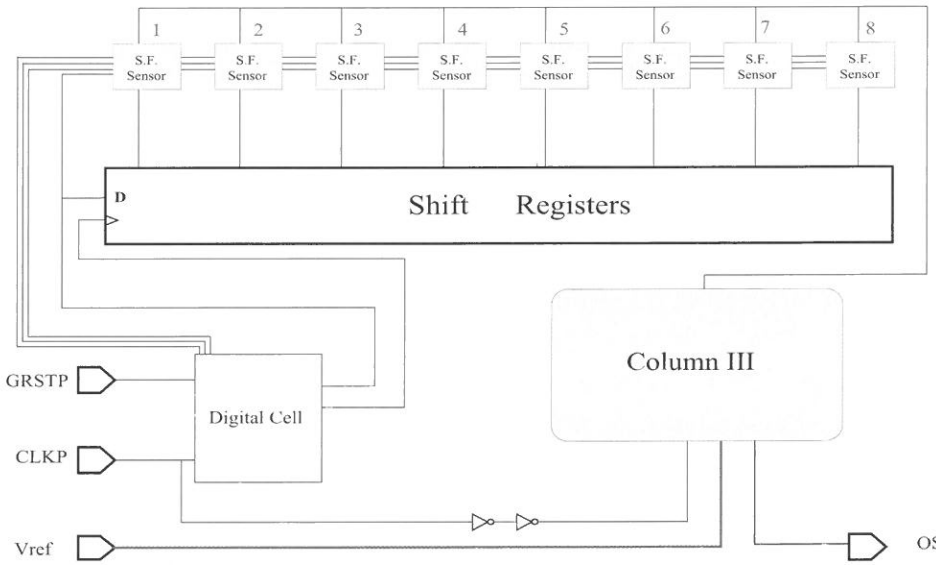

圖 22 一維影像感測器之方塊圖

如圖 23 所提出由 PhotoBJT 所構成的一維 PPS 架構的 CMOS 影像感測器電路 [9]，在沒有做 CDS 電路的情況下，每個 pixel 內部主要是透過 PhotoBJT 來做光電轉換，把累積到的 charge 經由 MOS switch 來傳送至 ODD/EVEN 的訊號線，最後再由放大器把訊號傳至輸出端 Vout。

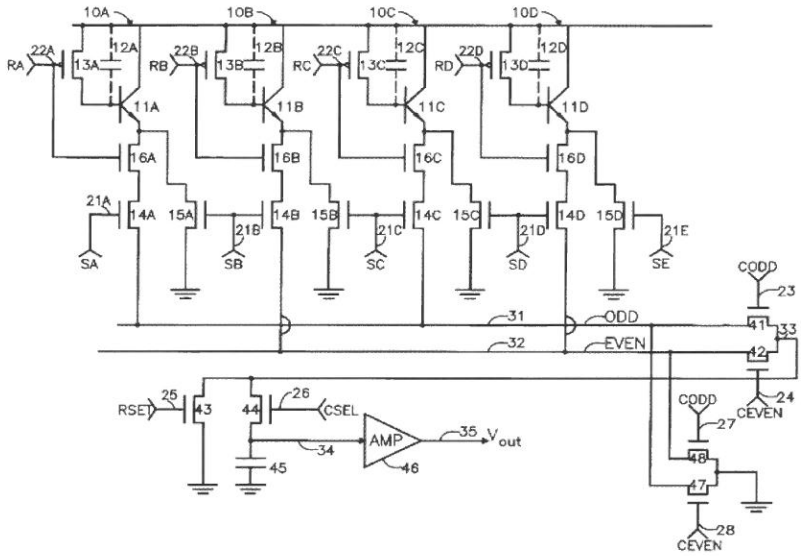

圖 23 PPS 架構的 PhotoBJT 感測線路

搭配著圖 24 的時序圖可以理解每個 PhotoBJT 皆是把 charge 傳送完成後，緊接著做 reset 動作，在第一個 pixel 內就是由 MOS 14A 及負緣的脈衝訊號 SA 來傳遞 pixel 1th 的 charge 至 ODD Video Line，而 RA 的低位準訊號會啟動 MOS 13A 來清除 Photo BJT 在 Base-Collector 所殘存的 charge 並把 base 端拉至最高電位 VDD，而緊接著第二個 pixel 的啟動時脈訊號 SB 一來，一方面 pixel 2 會把累積的 charge 傳遞到 EVEN Video Line，另一方面在 pixel 1 也會啟動 MOS 15A 來把 PhotoBJT 11A 的 emitter 端拉至 GND 電位，而讓 base 端能從原先的 VDD 降至近似於 0.5~0.7V，這個電位是 PhotoBJT 內部在 BE 介面的 Junction 位障電壓。從 RA → SB，才能完整的清除 PhotoBJT 11A 的殘存 charge，並且把 base 端拉至一個低的位準，以方便開始累積下一週期的光電訊號。依此類推，RB → SC 會完成 pixel 2 內部 PhotoBJT 11B 的清除動作，而 RC → SD 會完成 pixel 3 內部 PhotoBJT 11C 的清除動作。

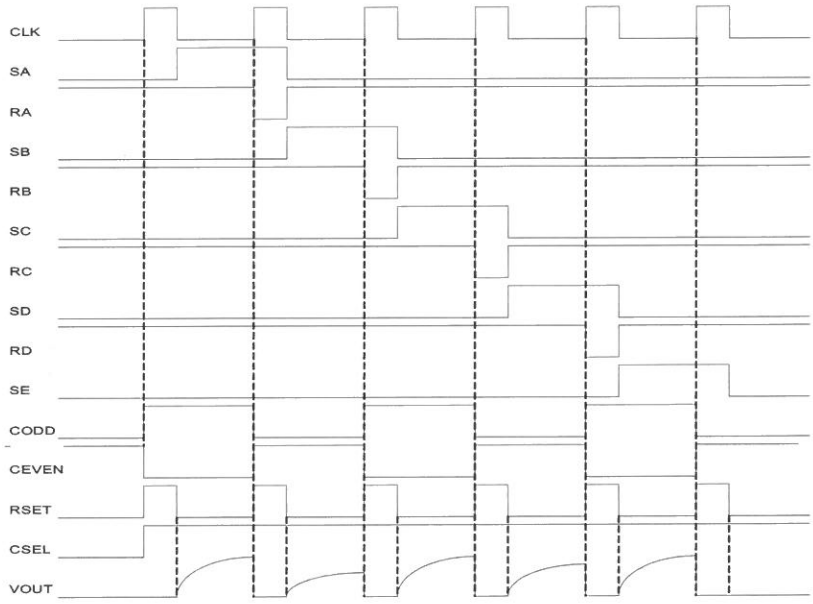

圖 24 PPS 架構的時序圖

至於在 ODD Video 和 EVEN Video 上的 charge 訊號會透過由 MOS41 和 MOS42 把兩者合成，並且電容 C 做充電的動作。最後透過 RSET 時脈及 MOS 43 和放大器 46 完成 charge 轉成電壓訊號的傳遞至輸出端 Vout。相比於 APS 架構，在 PPS 內每一個 pixel 少了兩個做 CDS 電路的電容，再者 PhotoBJT 比起 Photodiode 會有 β 光電流增益，這個優勢會讓 PPS 的放大器能使用較小的放大倍率，而達到最佳的速度。然而，在沒有使用 CDS 電路來消除 pixel 內部 MOS 所貢獻的 FPN 對於 charge 傳遞的訊號影響不大，且在於放大器使用近乎於 unit gain buffer 的操作，在最後輸出端的波形依然可以維持好的均勻度。在此 PPS 架構的讀取時間分別為

$$\tau_{PIXEL} = 5 \times (R_{on,M16A} + R_{on,M14A} + R_{on,M41A} + R_{on,M44A}) \times C \tag{11}$$

$$\tau_{AMP} = \frac{1}{A_{AMP}\omega_{0,AMP}} \tag{12}$$

τ_{PIXEL} 加上 τ_{AMP} 是決定整個一維 PPS 感測線路的讀取速度。由公式可知，整個 PPS 的讀取速度會被 τ_{PIXEL} 所限定住，原因是在信號傳遞路徑上有四顆的 MOS 當成開關串

接著，所以會拉慢信號傳遞的時間。此架構的 $Vo_{(sat)}$ 會是放大器的最大輸出電壓 = 1.0V, V_{noise} 約為 2~2.5mV，得到的 S/N 為 52~54dB。

在 APS 架構為了讓 FPN 能達到最小，在每一個 pixel 內部都會加上由兩個電容及四個 MOS 開關，不僅大大增加了 pixel 在 layout 上的面積，也降低了 fill factor，讓 Photodiode 能做光電轉換的面積變小。再者，在一維 PPS 架構中，為了達到完整的電荷清除機制，在信號路徑上串接了四顆 MOS，並且在每一個 pixel 內部皆有單獨的 reset timing 來啟動電荷清除之機制。雖然利用 PhotoBJT 先天俱有的電流增益來換取輸出端的放大器能使用近乎一倍的增益，讓 FPN 影響的程度能達到最小，在 pixel 的線路已經精簡為四顆 MOS 開關加上一 PhotoBJT，已經能改善 APS 上 fill factor 太小的缺點，不過，信號路徑上等效的四顆 MOS 開關，會降低信號的讀取速度。

在本論文中，吾人提一改良式的 PPS 架構如圖 25 和 26 所示，藉由 pixel 內部的 2 個 PMOS 電晶體和外部的放大器 (OTA) 來完成電荷清除的動作，並且把原先 PPS 架構裡在信號傳遞路徑上的四顆 MOS 減低為 2 顆 MOS，不但 pixel 的 fill factor 會被大大提高，在 pixel 內部也不需要複雜的時序來控制。

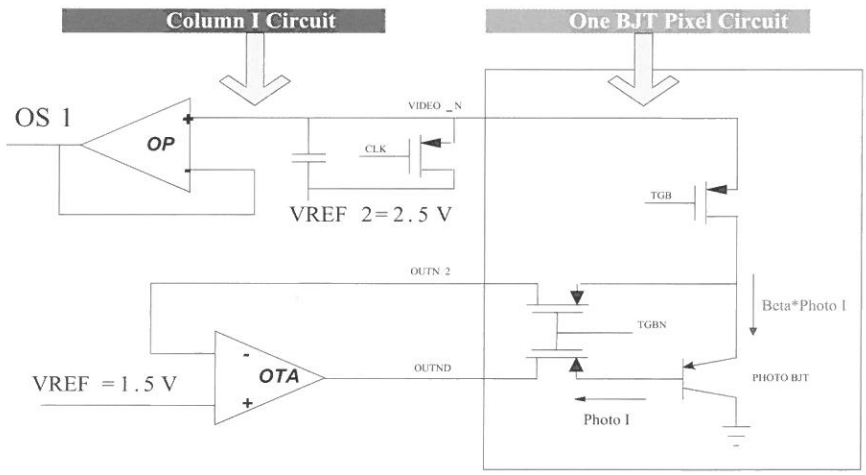

圖 25 所提新型 PPS 架構的 PhotoBJT 感測線路

在此 PPS 架構的讀取時間分別為 $\tau_{PIXEL} = 5 \times (Ron_{MTGBN} + Ron_{MCLK}) \times C_{VIDEO}$ 及 $\tau_{AMP} = 1/(A_{AMP}\omega_{0,AMP})$。$\tau_{PIXEL}$ 加上 τ_{AMP} 仍然是決定整個一維 PPS 感測線路的讀取速度。此架構的 $Vo_{(sat)}$ 會是放大器的最大輸出電壓 = 1.0V, V_{noise} 約為 2~2.5mV，得到的 S/N 為 52~54dB。

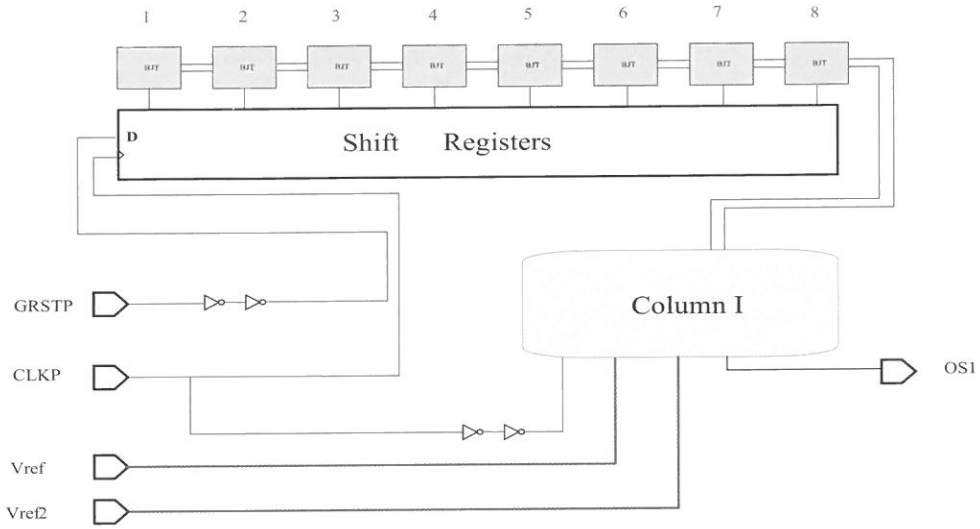

圖 26 所提新型 PPS 的架構圖

此外，針對新型的 PPS 架構能進一步把 PhotoBJT 串接成達靈頓對，如圖 27 所示，在 FPN 和單位增益的放大器使用相同條件下，由於達靈頓對有著 β^2 的電流增益，當被使用在相同的感測光源下能使得輸出端電壓大小獲得平方倍的提升。此電路可以使用和先前新型式 PPS 架構相同的時序控制和電路架構圖，也方便日後的驗證。

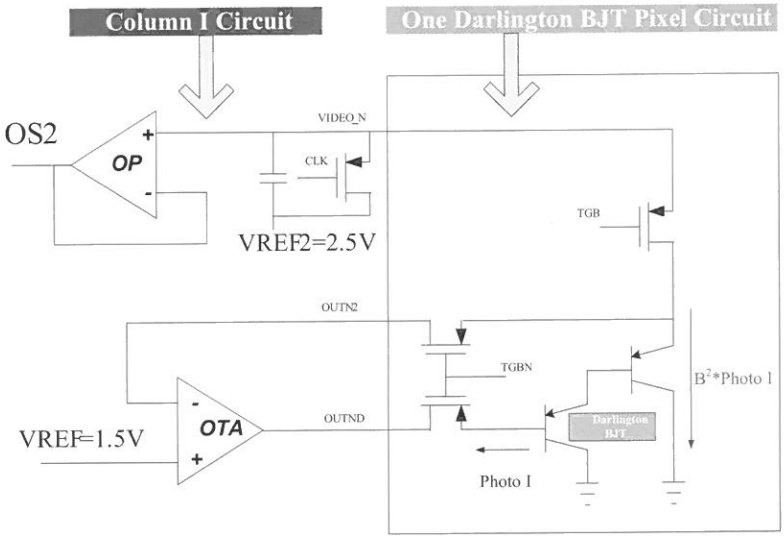

圖 27 新型 PPS 架構和達靈頓式 PhotoBJT 感測線路

3. 實驗結果與晶片量測分析

在晶片測試環境部份，利用如圖 28 所示的測試線路，在晶片上必須被蓋上一個不會透光的黑色塑膠殼，在 ALTERA 測試板上會提供二種數位控制信號 CLK 及 GRST 訊號後，可以直接透過程式界面來讀取晶片在照光和及不照光時的輸出值。此外，. 在黑殼上方有挖開一個洞並放上一單色 LED 光源，並利用程式來設定照光時間來量測晶片之輸出結果，來比較不同架構 APS 和 PPS 對光譜的反應。

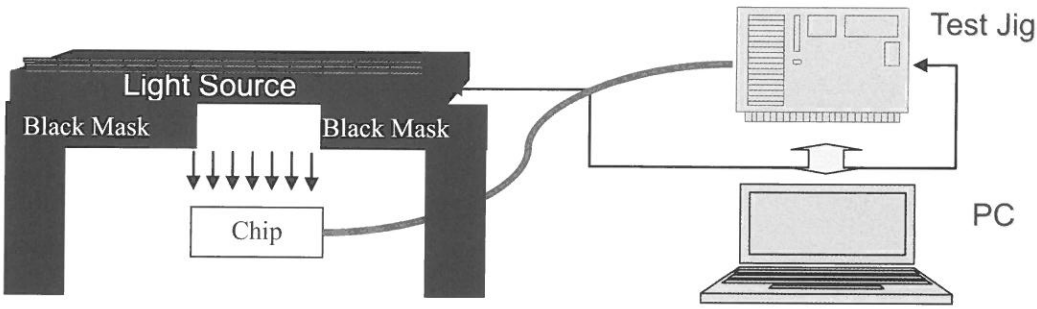

圖 28 晶片測試線路圖

新型 PPS I 架構在不照光量測如圖 29，其暗電壓為 2.406V, 當光源被調強且晶片輸出端呈現飽合波形輸出時如圖 30 所示，量測其動態範圍為 2.406-1.828=0.578V。另外在線性地調整光源條件量測方面如圖 31，新型 PPS I 的輸出也是呈現正常且線性的反應。

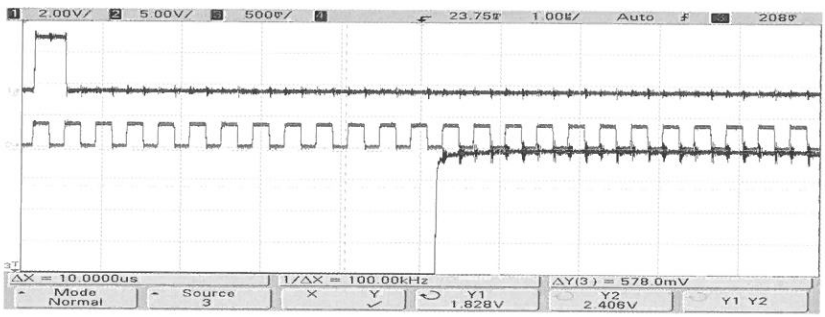

圖 29 新型 PPS I 在不照光條件的輸出波形

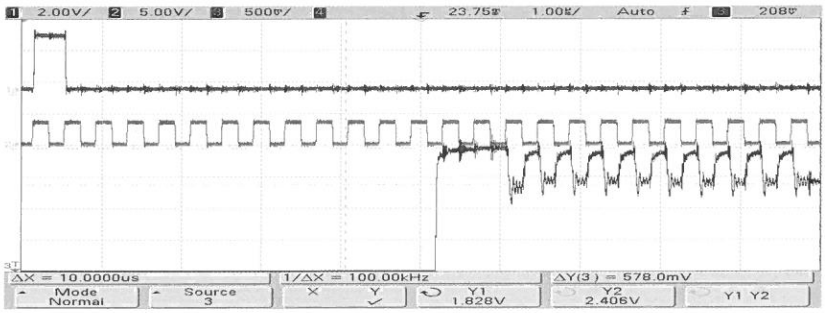

圖 30 新型 PPS I 在照光飽合條件的輸出波形

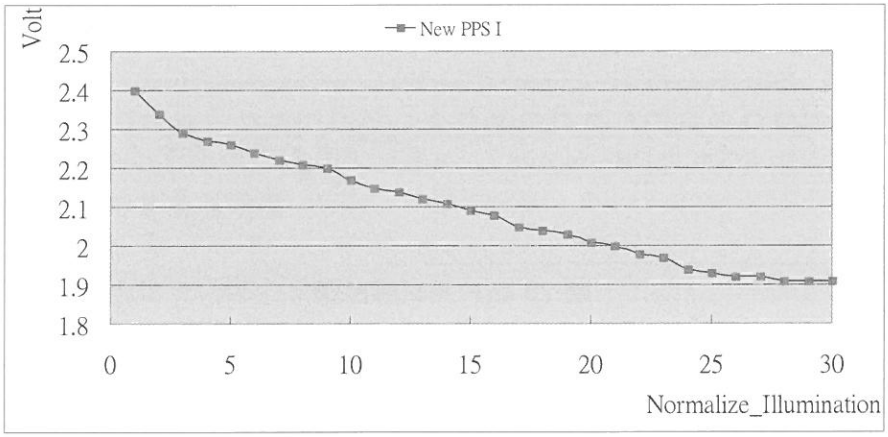

圖 31 新型 PPS I 在線性照光條件的量測

新型 PPS II 架構在不照光量測如圖 32，其暗電壓為 2.406V 和 PPS I 相同，當光源被調強且晶片輸出端呈現飽合波形輸出時如圖 33 所示，量測其動態範圍為 2.406-1.3768=1.03V。另外在線性地調整光源條件量測方面如圖 34，新型 PPS II 的輸出也是呈現正常且線性的反應。

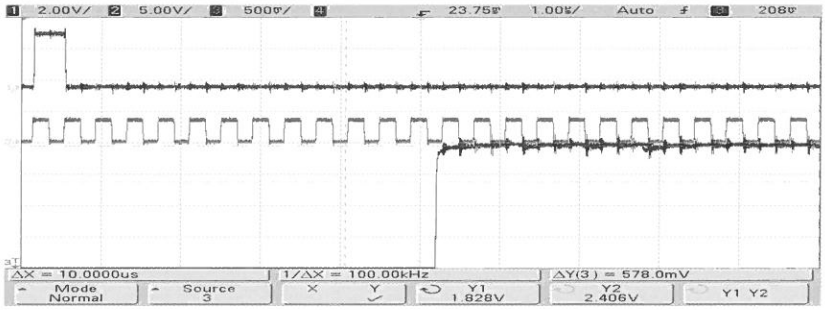

圖 32 新型 PPS II 在不照光條件的輸出波形

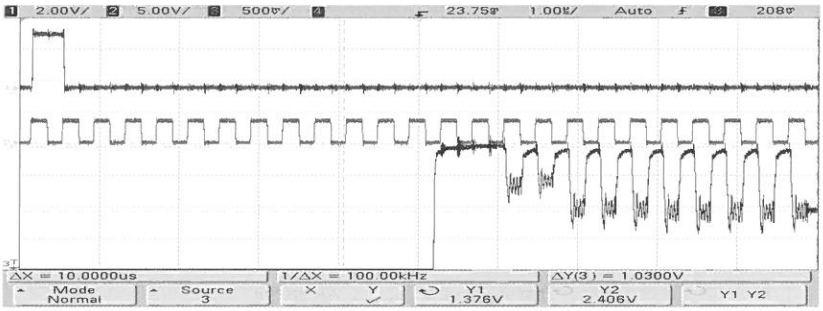

圖 33 新型 PPS II 在照光飽合條件的輸出波形

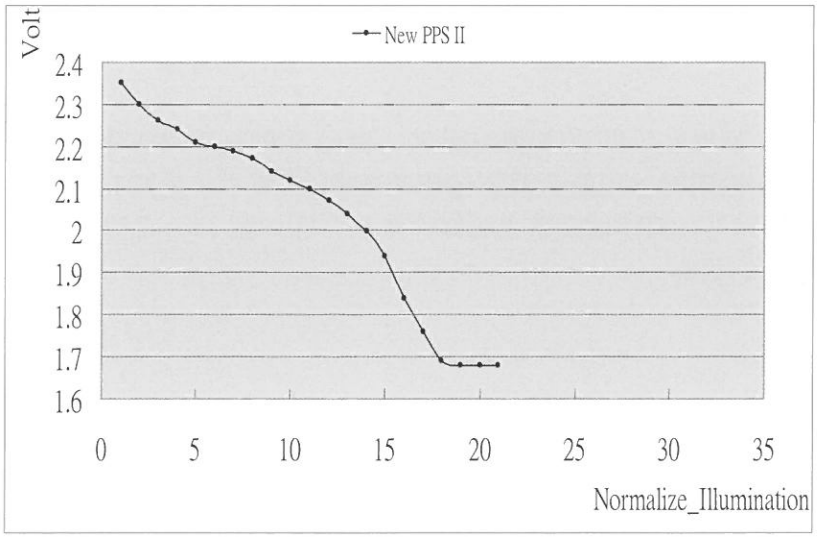

圖 34 新型 PPS II 在線性照光條件的量測

關於 spectrum 的量測如圖 35 所示，由於使用相同的 PNP10 元件，所以在 PPS I 和 PPS II 在 spectrum 量測會得到近似的結果。

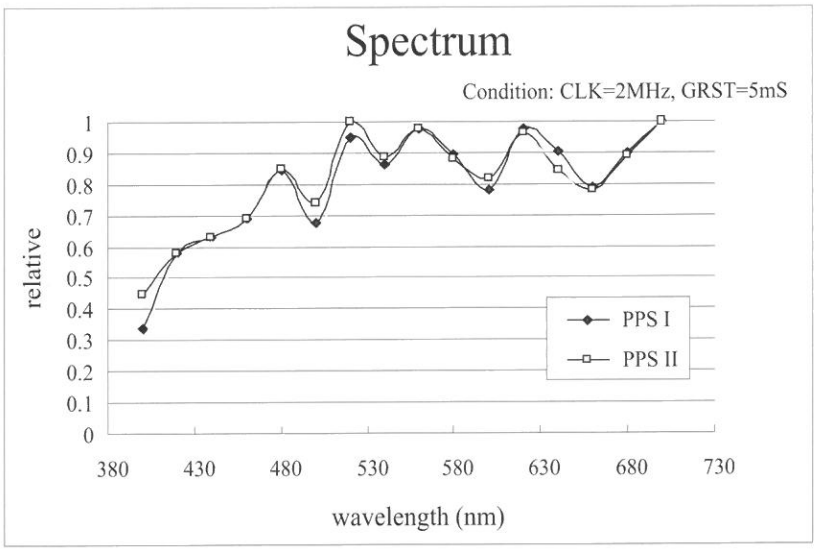

圖 35 Spectrum 的量測

如表 2 是整理 PPS I 和 PPS II 兩者之量測數據比較表。

表 2 量測規格一覽表

規格	量測結果	
Pixel Sturcture	PPS I	PPS II
Photodectector	PhotoBJT	Darlington BJT
Supply Voltage	3.3V	
Data Rate (CLK rate)	2.5MHz	
Per line Speed	6ms	
Sensor Resolution	2400DPI	
VREF	2.1V	
VREF2	2.4V	
Power consumptions	2.1mA × 3.3V, 6.9mW	2.15mA × 3.3V, 7.1mW
Saturation Voltage	0.578V	1.03V
Random Noise	2.2mV	2.6mV
S/N ratio	48.4	51.9
Linearity	Straight Line	Two Segment Line

4. 結論

近年來在 CMOS 影像晶片之類比前端電路，主要還是以光感測器 Photodiode 加上 Source follower(3T) 的 APS 架構為主。多數論文研究皆是以此 APS 架構做類比對數位轉換，或者是以交換式電容的方式來提升整個影像惑測器的 S/N 比。然而本論文主要是以 PhotoBJT 加 switch(3T) 新型式的 PPS 前端電路為主，利用 PhotoBJT 先天俱有的電流增益 (β) 來取代傳統 APS 架構裡的 Source follower，並且在 Column 電路加上 Reset switch 及外部 OTA 組成的 feedback reset loop 來減少原先在 APS 架構裡 MOS 的 size 和數目，使得像素裡的 fill factor 能達到最高，進而得到高 S/N 比。

根據矽晶片的量測結果，在 Linearity 的量測也驗證，PPS I 是相當線性的，不過在 PPS II 因為是採用二顆 PhotoBJT 串連的方式，會有兩種不同斜率的線性曲線，一段斜率為 β 的直線，而另一段是斜率為 β^2。功率量測方面，在放大器使用較少的 PPS I 和 PPS II 會較省電。此外，本論文在經由晶片之量測結果證明，由 Photobjt+3T Switch 的 pixel cell 架構具有低消耗功率及高 S/N 比之特性，適用於操作高速之影像晶片之類比前端電路。

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Design and Implementation of High-Speed CMOS Analog Front-End Circuits for Image Sensors

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Abstract

With the proliferation of digital cameras and multi-functional printers, document scanning has become much more easily. Image processor IC's have been popular consumer electronic products. The core image processor IC's can be classified two catalogs: one is based on CMOS technologies and the other is with CCD architecture.

The two factors, price and resolution actually determine the applications of the two image processor IC's. The CCD based image IC's have the advantages of high S/N and large dynamic range, which therefore are employed in the products of high resolution and high scan speed. By contract, CMOS based image IC's are used in low-resolution and low-speed products.

This paper is aimed at investigating image sensors in CMOS and CCD technologies, we also present the analog front-end readout circuit design specifications of CMOS image IC's. Meanwhile, we also propose a novel architecture of the readout circuits to improve the S/N of CMOS based image IC's, which we expect the proposed architecture can be applied in high-resolution and high-speed image circuits.

Key words: image processing, analog front-end readout circuits, dynamic range.

Generalized Active Immittance Simulator using Differential Voltage Current Conveyors

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Abstract

In this paper, a generalized active immittance simulator circuit using three differential voltage current conveyors (DVCCs) and three passive components is presented. Depending on the passive elements selection, the proposed circuit can realize synthetic floating inductor and floating frequency-dependent negative resistor (FDNR). The unique features of this circuit offer the following advantages: (i) No requirement on component matching for the desired schema; (ii) Independent control of immittance value facilitated through two resistors. For the application, the inductor in the LCR passive filter circuits can be replaced by the proposed floating inductance simulator. Thus, the advantages of these new active RC filters without an inductor can include low component sensitivities and utilize the extensive capability of the primary LCR filter design. In order to show the performance of the proposed immittance simulator circuit, a second-order voltage-mode RLC passive bandpass filter is experimentally demonstrated. The ideal simulated and experimental results of the filter confirming the theory are included.

Key words: differential-voltage current conveyor, inductor simulators, analog circuit design, active filters

1. Introduction

Active filters are widely used in signal processing. Many circuits employing the second-generation current conveyors (CCIIs) or the four-terminal active current conveyors as active elements for current-mode filters, voltage-mode filters, sinusoidal oscillators and immittance function simulators have been presented earlier [1]~[19]. For example: Chang presented a single input and a single output current-mode filter using one CCII [7~8]. Chang proposed a universal current-mode filter with three inputs and one output [9]. Senani employed seven CCIIs, two capacitors and three resistors to realize a single input and three outputs filter [10]. Yin realized a one input and three outputs current-mode universal filter employing five CCIIs, three capacitors and two resistors [12]. Senani employed only a single CCII along with a single capacitor and two resistors to realize a circuit for the simulation of a parallel floating- inductor and resistor (parallel RL). This circuit does not require matching components [12]. Singh used a single CCII, a single capacitor and two resistors to simulate a lossy floating inductance series resistor (series RL), with no component-matching requirement [13]. Senani proposed two new active RC networks, employing two CCIIs, a single capacitor and four resistors, to realize series/parallel RL impedance, with no element matching conditions [14].

A recent publication introduced a versatile active-circuit building block termed differential voltage current conveyor (DVCC). It was constructed by Pal [20] and then was developed and realized in CMOS technology by Elwan and Soliman[21]. The DVCC has become very popular because of its high signal bandwidth, great linearity and large dynamic range. Therefore, it has been useful in many analogy signal processing applications to general all-finite linear circuits and applied in the areas of oscillator design, active filters, and cancellation of parasitic elements [20]~[29]. For example: Elwan and Soliman employed two DVCCs and two capacitors to synthesize current-mode bandpass and lowpass filters [21]. Ibrahim, Minaei and Kuntman used three DVCCs and six passive elements to construct current-mode Kerwin uelsman ewcomb biquad [25]. Yin employed two DVCCs and some passive components to construct bandpass, lowpass, notch, allpass and highpass filters [26]. Yin used a DVCC and some passive elements to realize lowpass, bandpass and highpass filters [27][28].

For the application, simulated immittance can be applied in the area such as oscillator design, active filters and cancellation of parasitic elements. The designing active filters by simulating the inductor of a passive LCR realization of the filter include low component sensitivities and the ability to utilize the inherent advantage of LCR filter design.Therefore, the LCR passive filters with simulated immittance have also received considerable interest. For example: Yin used two DVCCs as active elements and three passive elements to synthesis the grounded inductance, grounded capacitance and negative resistor simulation circuit in 2012[29]. The proposed grounded inductor simulator of [29] is applied to replace the grounded inductor of the RLC passive filters. Thus, the new RC active filters can enjoy the advantages of the RLC filters. Unfortunately, the floating inductor of the RLC passive filters can not be transferred to RC active filters by the proposed grounded inductor simulator. For this reason, the simulated floating inductor need be constructed to solve the mentioned problem.

In this study, a new circuit configuration for the simulation of floating inductance and FDNR using two DVCCs and three passive components is proposed. The proposed floating immittance simulator circuit has no passive component matching condition imposed. As an application sample, the simulated floating inductor is used to replace the floating inductor of the LCR passive filters. Moreover, the new RC active filters can enjoy low component sensitivities and extensive knowledge of LCR filter design and benefit from the LCR passive filters. Finally, the series LCR passive bandpass filter using the proposed simulated inductor is experimentally validated.

2. CIRCUIT DESCRIPTION

The circuit symbol for a DVCC is shown in Fig.1. The port relations of a DVCC can be characterized as $V_x = V_{y1} - V_{y2}$, $I_{Z+} = I_x$, $I_{Z-} = -I_x$ and $I_{y1} = I_{y2} = 0$. The '+' and '-' signs of the current i_z denote the non-inverting and inverting, respectively.

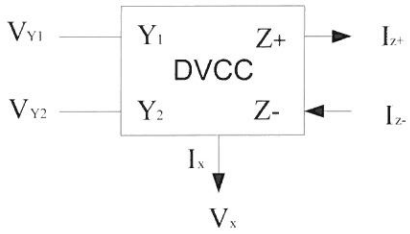


Fig.1. A DVCC symbol

The active immittance simulator circuit is shown in Fig.2, where Z_1~ Z_3 are impedances. By routine analysis, one get, for the circuit of Fig.2, the input impedance of the active immittance simulator equation is given by

$$Z_{in}=\frac{Z_1 Z_3}{Z_2} \quad \text{.....(1)}$$

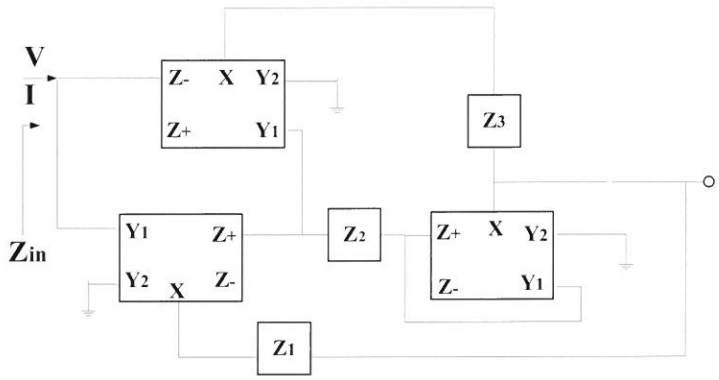


Fig.2 The proposed floating impedance simulator.

By choosing suitable passive components from the impedances Z_1, Z_2 and Z_3 in equation (1), the floating inductors and floating frequency dependent negative resistors can be obtained as follows:

(1) If $Z_1=R_1$, $Z_3=R_3$, and $Z_2=(1/sC_2)$, are taken, the impedance of the floating inductor is obtained as

$$Z_{in}=sL_{eq}=s\,C_2R_1R_3 \quad \text{.....(2)}$$

where $L_{eq}= C_2R_1R_3$. The sensitivities of the active inductance are

$$S_{C_2}^{L_{eq}} = S_{R_1}^{L_{eq}} = S_{R_3}^{L_{eq}} =1$$

From the above equation (2), properly selecting values of the resistors and capacitors, both large and small values of inductance and capacitance can be obtained. Thus, the floating inductance simulator is constructed and its values are independently tunable through the three passive elements in the circuit of Fig. 3.

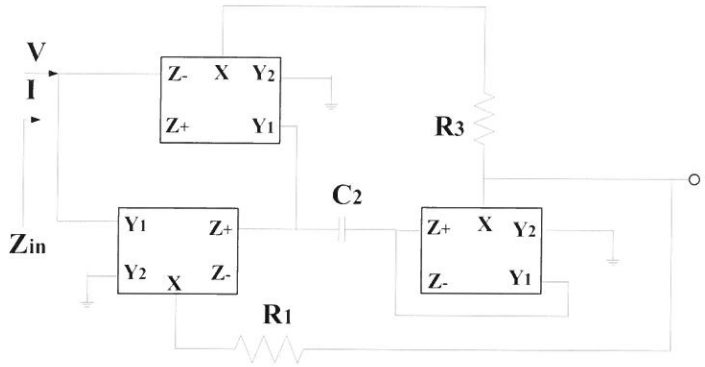


Fig.3 The proposed floating inductance simulator.

(2) If $Z_3 = (1/sC_3)$, $Z_1 = (1/sC_1)$, and $Z_2 = R_2$, are taken, the floating FDNR is given by

$$Z_{in}=\frac{1}{sD_{eq}}=\frac{1}{s^2C_1C_3R_2} \quad \text{.....(3)}$$

where $D_{eq}= C_3C_1R_2$. The sensitivities of the active FDNR are

$$S_{C_1}^{D_{eq}} = S_{C_3}^{D_{eq}} = S_{R_2}^{D_{eq}} = 1$$

Similarly, the floating FDNR simulator can be obtained and its values are independently tunable through the three passive elements.

3. SIMULATION AND EXPERIMENTAL RESULTS

The AD844, as integrated circuit, is now commercially available. The DVCC is implemented by three ICAD844s, three IC op-amps and five resistors. The theoretical characteristic of the FDNR, described in Fig.2, is given for C1= C3=1 μ F and R2=10kΩ.

The Matlab analysis is proven to be effective when the optimum curve of the FDNR circuit is applied shown in Fig.4. It is observed from equation (3) and figure 4 that the impedance of the FDNR decreases with increasing frequency.

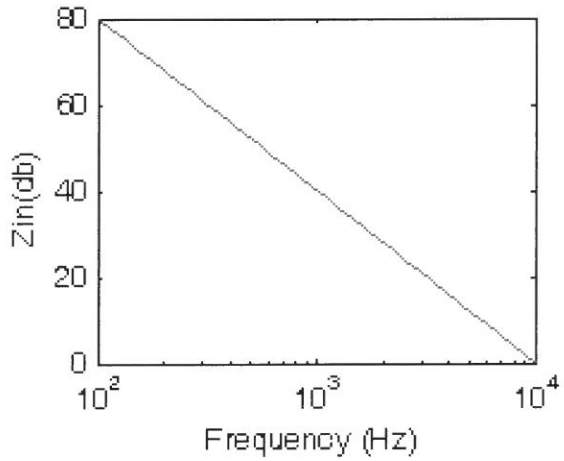


Fig.4: The ideal curve of the FDNR for C_1= C_3=1 μ F and R_2=10kΩ.

If the proposed simulation floating-inductor was experimentally tested using $R_1 = R_3 = 1K\Omega$, $C_2 = 1\mu F$ and IC AD844s, the proposed circuit shown in Fig.3 can be equivalent to an inductor with $L_{eq} = 1H$.

Then, this simulation floating-inductor can be used in the realization of the series RLC passive bandpass filter shown in Fig.5 and the transfer function has a biquadratic bandpass characteristic with

$$\frac{v_{out}}{v_{in}} = \frac{(\frac{R}{L_{eq}})s}{s^2 + s(\frac{R}{L_{eq}}) + \frac{1}{L_{eq}C}} \quad \text{.....(4)}$$

the central frequency: $\omega_o = (\frac{1}{L_{eq}C})^{1/2}$ .....(5)

the quality factor: $\vartheta = R(\frac{L_{eq}}{C})^{1/2}$ .....(6)

The sensitivity of o and according to passive components are:

$$S_{C_2}^{\omega_o} = S_{R_1}^{\omega_o} = S_{R_3}^{\omega_o} = S_C^{\omega_o} = S_C^{\vartheta_o} = -\frac{1}{2},\ S_{R_1}^{\vartheta_o} = S_{R_3}^{\vartheta_o} = S_{C_2}^{\vartheta_o} = \frac{1}{2},\ S_R^{\vartheta_o} = 1$$

all of which are small.

Fig.5 The prototype passive series RLC bandpass filter

In Fig.6, a second-order bandpass filter was constructed with $R = 1K\Omega$, $C = 1\mu F$ and $L_{eq} = 1H$. The Matlab has simulated the ideal curves of the bandpass filter. The measured values were found using a Hewlett Packard network/spectrum analyzer 4195A. The resonance frequency was monitored and measured and the corresponding inductance value was calculated and compared with the theoretical value calculated using equation (2). The experimental results for the gain and phase responses shown in Fig.7 (a) (b) demonstrate similarity between theoretical calculation and actual measurement. There is a high correlation between the theoretical analyses and the measured results with only minor errors due to the use of passive elements.

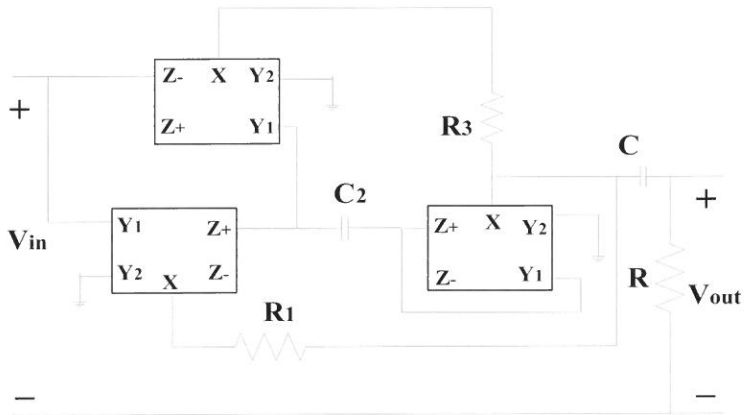
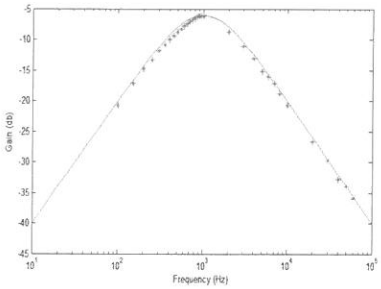
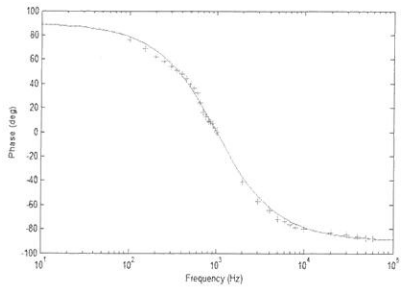


Fig.6 Bandpass filter circuit used to test the inductor realized using circuit of Fig. 4



(a)The gain response curve of the banspass filter using simulated inductor.



(b)The phase response curve of the banspass filter using simulated inductor.

Fig.7 (a): The gain response curve of the banspass filter using simulated inductor.
(b): The phase response curve of the banspass filter using simulated inductor.
*: Experimental result for banspass gain
+: Experimental result for bandpass phase
—: Ideal curve

4. CONCLUSION

The concept of the floating inductor and FDNR using three DVCCs and three passive elements is proposed. The inductance value of the proposed circuit can be independently tunable through the three elements - R_1, R_3 and C_2, and it does not require matching of any passive component. The advantages of RC active filter when constructing filter transferred by the proposed circuit includes low component sensitivities and the ability to utilize the extensive capability of LCR filter design. Finally, the experimental results on floating inductor utilizing a LCR bandpass passive filter confirmed the theoretical analysis.

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使用差動電壓電流傳輸器合成一般化主動阻納模擬器

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摘　要

本文提出使用差動電壓電流傳輸器當主動元件，合成一般化主動阻納模擬器。此一般化主動阻納模擬器，有許多利益。其一是：沒有任何元件匹配要求；其二是：模擬浮接式電感值可以經由兩個電阻分別獨立調整；其三是：可以合成相依頻率負阻抗電阻。電感模擬電路的好處是，可以用來取代現有被動濾波器的電感值，使其可以被製作成積體電路，同時被動濾波器既有的優點，在被轉換成主動濾波器後，這些優點仍可繼續存在。最後，本文以既有的串接式二階被動帶通濾波器，應用本文所提出的電感模擬電路取代其電感值，以驗證本文之理論預測。

關鍵字：差動電壓電流傳輸器，電感模擬器，類比電路設計，主動濾波器。